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How do Mechanics and Thermo mechanics affect microelectronic products: Some residual stress and strain effects, investigations and industrial management.

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How do Mechanics and Thermo mechanics affect microelectronic products:
Some residual stress and strain effects, investigations and industrial management.

Abstract

The work reported here aims to provide to the reader some features on several items related to the microelectronic industry. The content is built in order to, even for non expert of the semiconductor fields, allow a comprehensive understanding of the technology development problematic. Its range from general considerations, to applications and researches on mechanical challenges. These later have been investigated in the last few years within STMicroelectronics.

Hence, starting from a general description of the microelectronic device market, the main processes of chip manufacturing are depicted. Then, focus is put on mechanical and thermo mechanical phenomena occurring during manufacturing and qualification tests. Challenges of such mechanisms are presented, and the need for a deep understanding of the physics is highlighted.

Requirements for numerical tools, and the industrial context, are justified underlining the need for smart compromises.

Specific numerical methods have been developed, implemented and tested. Results have been faced to experimental results for correlation purposes, allowing additional insights and virtual prototyping.

This work proposes, trough a selection of applications, to briefly show results on FEoL, BEoL and packaging features of the device. Extracted from team publications, typical examples of strain engineering and fracture mechanics investigations are presented. Their added values are highlighted.

This thesis would help people to get familiar with some methods to deal on mechanical and thermo mechanical topics in a technology development framework of the microelectronic industry.

Key-Words: Microelectronics, simulation, thermo-mechanical stress, strain engineering, piezoresistive boosters, fracture mechanics, energy based failure index, multi-scale, homogenization.

Impacts mécaniques et thermomécaniques dans les produits de la microélectronique : Effets des contraintes résiduelles et déformations, recherches et développements de méthodes numériques dans un cadre industriel.

Résumé

Ce document propose au lecteur quelques éclairages sur l'industrie de la microélectronique : Il doit permettre à un public non expert du domaine des semi conducteurs une large compréhension des problématiques mécaniques et thermomécaniques rencontrées lors des développements technologiques des produits. Aussi, des exemples techniques spécifiques sont choisis. Ceux-ci illustrent des travaux de recherches appliquées visant à répondre aux besoins industriels de la course à la miniaturisation et l'amélioration des performances.

En première partie les généralités du marché, les grandes tendances technologiques, ainsi que les procédés de fabrication sont décrits.

L'attention est portée ensuite sur les phénomènes d'origines mécaniques qui se manifestent durant l'élaboration ou la qualification des puces. Les challenges à relever, les compromis à concéder dans un cadre industriel concernant les besoins numériques et expérimentaux pour faire face à ces problématiques sont soulignés.

Enfin, quelques travaux internes de développement d'outils numériques et leur application sont illustrés par des exemples. Des stratégies de simulations particulières, incluant des modélisations multi échelles, techniques d'homogénéisation et calcul d'index de défaillance énergétiques dédiés, permettent d'une part d'améliorer la compréhension des physiques mises en jeux et d'autre part d'optimiser les architectures. L'usage quotidien de ces travaux contribue à l'amélioration des performances électriques et la diminution des pertes de rendement. En fournissant des règles dans les phases amonts de conception des architectures, les temps de mise sur le marché de nouveaux produits et leurs coûts de développement sont ainsi diminué.

Mots-clés : Microélectronique, simulation, contraintes thermomécanique, ingénierie des déformations, effet piezorésistif, mécanique de la rupture, critère de défaillance énergétique, multi échelles, homogénéisation.

How do Mechanics and Thermo mechanics affect microelectronic products: Some residual stress and strain effects, investigations and industrial management

1 Introduction and generalities about microelectronic industry

The frame of this work is to present in a general way some mechanical and thermal topics in the microelectronic industry.

At first, some generalities of the semiconductor fields will be described: History, trends, technological and manufacturing details will be depicted. Then, focus will be made on technical considerations, more precisely, mechanical and thermo-mechanical concerns on devices will be particularly illustrated. Hence, chapters will be scoped on stress and strain related questions occurring during products manufacturing and qualifications.

This would help to answer on how to deal with stress issues in the technological development fields, both for electrical performance and yield purposes? Highlights will be made on modeling methodologies which have been specifically developed during the past few years at STMicroelectronics. These are used in order to understand manufacturing processes, and help technology development and product designs. Ultimate goals of such works are to save time and reduce costs of manufacturing.

1.1 Technological trends: The "Moore" and "More Than Moore" laws.

As a starting point to depict some semiconductor generalities and related scientific frames, the Moore Law (Figure 1) is commonly used to describe the performance improvements and critical dimension evolutions of the transistors. This formalizes the densification feature of the device by area on a chip. Consequences of geometrical decreases are huge and lead to the need for the industry to constantly keep efforts on innovations, thus on financial investments on research, development and production tools.

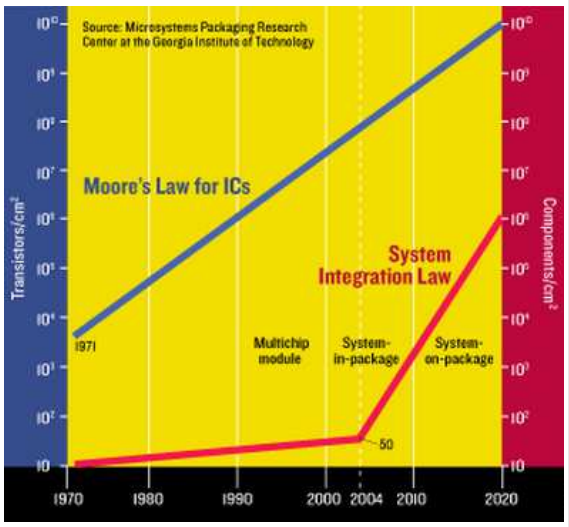


Figure 1 "Moore principle" [International Technology Roadmap for Semiconductors http://www.itrs.net/]

In parallel, the derived "More than Moore" law (Figure 2) has been proposed to denote the fact that race for miniaturization is now reaching its limitations. More precisely, it underlines that, as an alternative to critical dimension downscale, the development of integrated systems would be a solution to stick with the performance specification challenges.

This later consideration leads to a major turn for many fields of the semiconductor industry. The narrowing of the gap between front-end and back-end manufacturing processes is a typical example of the new challenges of the electronic market and design tools. Figure 3 shows the envisaged future for devices and systems. Contrasting with past designing, systems are more and more integrated into a single part. To achieve such integrations, novel processes and technologies need to be conceived. Beyond the core CMOS downscaling, the industry is facing new paradigms.

The last sections of this thesis will be dedicated to the near and mid terms future of technological trends introducing three dimensional integration, which becomes one of the main frame and work direction to fit device performance roadmaps.

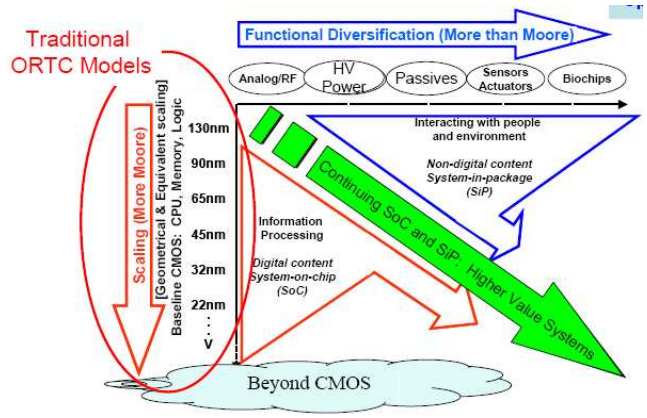


Figure 2 "More than Moore principle" [International Technology Roadmap for Semiconductors http://www.itrs.net/]

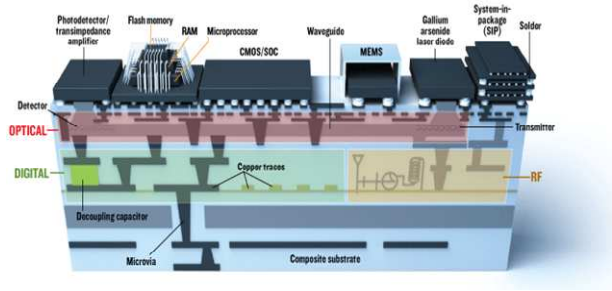


Figure 3 From "More" to "More than Moore": System integration.

1.2 Manufacturing: FEoL, BEoL, assembly and packaging process groups

Producing an electronic device is based on a huge amount of steps while chips are batch processed on un-diced silicon wafers. Aiming to reduce costs, wafer sizes are constantly increasing. More precisely, standard wafer diameter was around 150mm in the mid 1980, and 300mm is currently used. Upgrades to 450mm diameter remains questionable for integration and production efficiency. Evolution of this feature, exposed in Figure 4 through years, is a constant question and is a result of a compromise between manufacturability, process feasibility and development costs which are inherent to the wafer size.

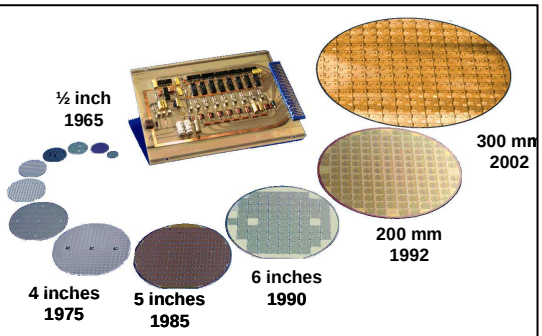


Figure 4 Wafer size trends [A History and Overview of the International Technology Roadmap for Semiconductors (ITRS) For the DOE Solid State Lighting (SSL) Program Planning

Manufacturing steps are usually split in wide families (Figure 5):

Starting from a silicon mono crystal, firstly diced to commonly 750 µm thick, the front end of line (FEoL) consists in the stages that allow making the core electrical functionalities into the silicon. After contacting the transistors together, comes the back-end of line (BEoL), which resides in building

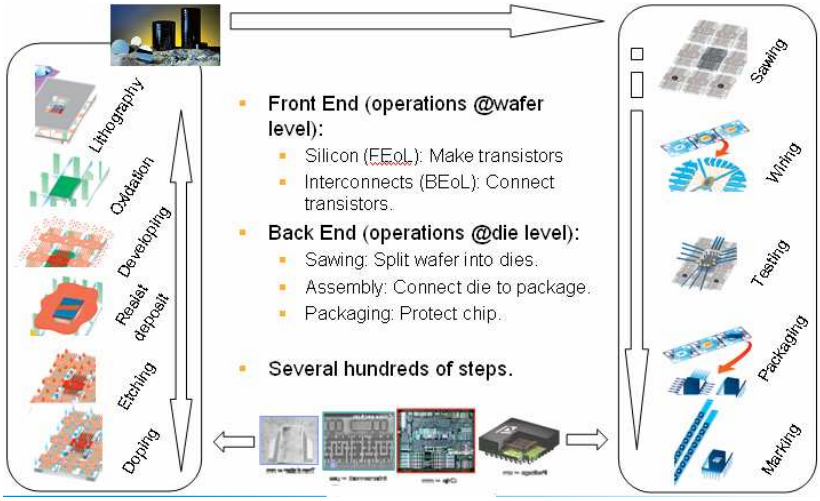


Figure 5 Schematic manufacturing process flows.

copper lines in isolator to assume the connection of the transistors: These floored wires, surrounded

by dielectrics, i.e. the insulating materials, are called the interconnections. In order to save room and optimize silicon surface usage, back-end connections use tri dimensional designing, as shown in Figure 6.

From the mechanical point of view, this region requires a particular attention.

Indeed, specifically due to the recent introduction of brittle dielectric materials, several kinds of mechanical and thermal failures locate in BEoL Most parts of this PhD will be interested in this region.

Once FEoL and BEoL process steps are achieved, manufacturing stages consists in establishing connection in between the electrical blocks previously created. Then, the assembly processes ensure the first external connection of the chip to the package.

Several options are available and, after the die to be tested (Figure 7), diced and thinned, the wire bonding (Figure 8), flip chip bumping, copper pillar bumping are respectively the most used assembly processes. These allow the mount ability of the chip into the final product.

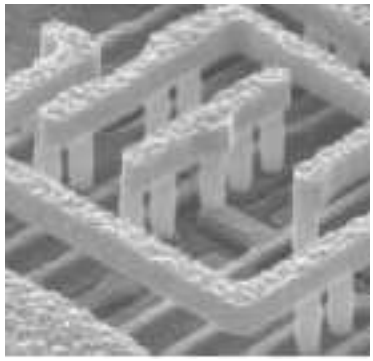
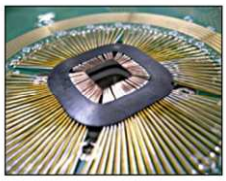


Figure 6 BEoL: Unprocessed interconnections (dielectric removed), 3D view of copper lines and tungsten contacts.



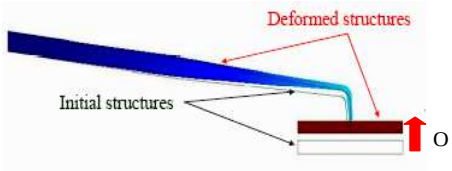


Figure 7 Probe card and probing process.

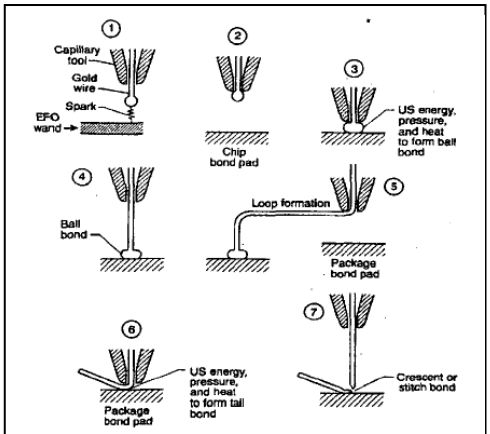
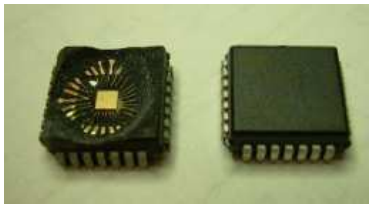


Figure 8 Wire bonding process.

Finally silicon chip and its substrate are then molded (Figure 9) for protection purpose with respect to "real life" product, and to ensure its isolation with respect to the external environment.



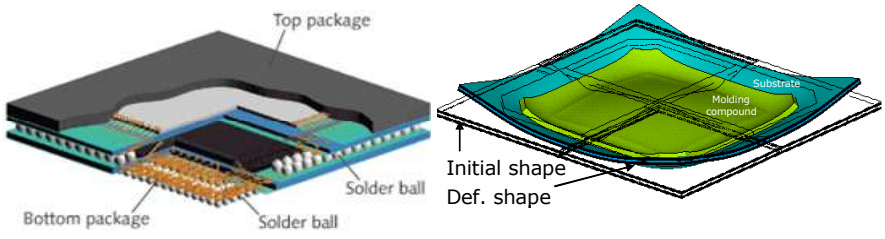


Figure 9 Die-Package encapsulation

1.3 Product qualification, maturity concept

Beyond the manufacturing processes themselves, device integrity must be further ensured. For that purpose, while developing technologies, integrity checks are performed at several stages with specific test cases. Life time sensitivity is precisely monitored, and products are tested within dedicated conditions of temperature, atmosphere, pressure, electrical and mechanical loading.

These tests are internationally standardized; on the other hand, rules severities are distinguished depending on the final device segment (automotive, communications, multimedia, health care, defense, etc.). The JEDEC organization is the leading developer of standards for the solid-state industry [http://www.Jedec.org]

Depending on tests and yield results, maturity grades of the technology are granted. Maturity levels are sorted with respect to the process and design settings that are left under definition, and also serve to allocate the acting teams of new product introductions (Figure 10).

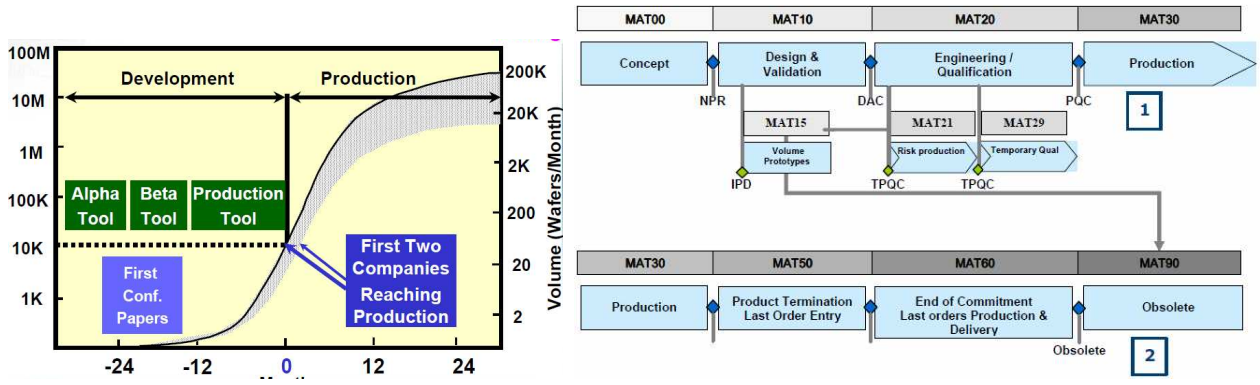


Figure 10 Technological development, product volume ramp up (left). Maturity milestones (right): (1) From growth to production (2) From saturation, decline and obsolescence [ST sustainable excellence N15]

2 Mechanics in microelectronics

Following the aforementioned generalities on semiconductors, the next sections will be focused on mechanical related topics. Target is to point out some stress related mechanisms, inducing either benefits or damages to the device performance or integrity. Through manufacturing processes, some key contributors of strain will be presented.

2.1 Typical strain & stress contributors

2.1.1 High temperature deposits and CTE mismatch.

Most of the process steps are high temperature full sheet deposited thin films. Maximum temperatures are usually higher in FEoL and can reach, at least in a short time pulse, of about 1000°C. As for the BEoL operations, temperatures are kept under 400°C to save global thermal budget.

Since the coefficient of thermal expansion of the films are commonly not equal to the previously built up substrate, the cooling back to ambient temperature induces stress within layer and substrate. The force balance leads to both partial stress relaxation of thin film, and wafer curvature (Figure 11).

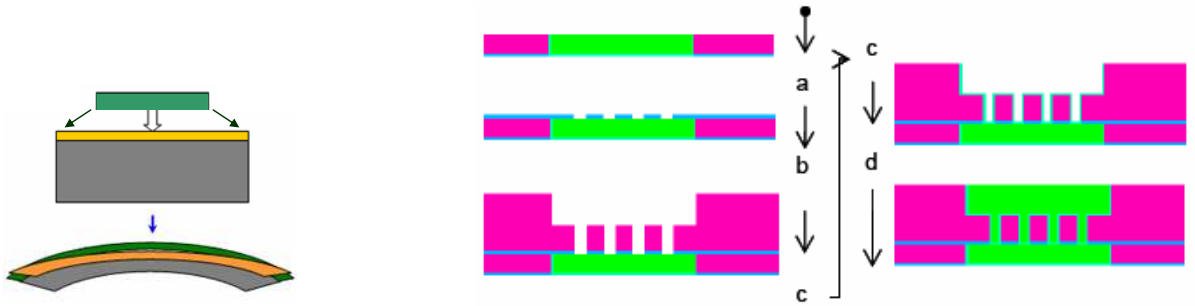


Figure 11 Left: Scheme of wafer bending induced Coefficient of Thermal Expansion (CTE) mismatch and high temperature deposit. Right: Dual damascene process.

The hence induced stress is named "residual", which includes both thermo mechanical and intrinsic film deformations.

2.1.2 Off balance deposits

In addition to the aforementioned phenomena, thin films are susceptible to lye on the substrate in a non balanced state. Consequences are similar to the previous mechanisms, and the generated strain is named "intrinsic" stress. The intrinsic stress is closely managed by the atomistic affinity in between the deposit layer and the adhesion with the substrate.

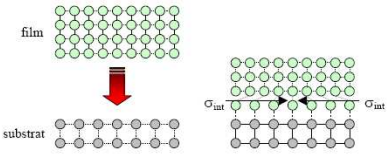


Figure 12 Schematic of Intrinsic stress generation due to off-balanced deposit

2.1.3 Non linear and relaxation mechanisms

Finally, during the next steps of the process flow, material structure and mechanical properties are changing and non linear phenomena are observed. These are usually stabilized within a couple of thermal cycle while materials are cured. Material behaviors can here be considered, in a first approach, as thermo mechanically linear response. However, it must be noticed that the final properties of the films are strongly dependent of many factors such as process conditions, annealing, patterning and shape features. On the other hand, the scale of interest, which is in the order of the microstructure size, contributes to complex physic mechanisms. As a consequence from the modeling point of view, simplifications need to be made, and assumptions must be considered with care to ensure both feasibility of simulations and result relevancies.

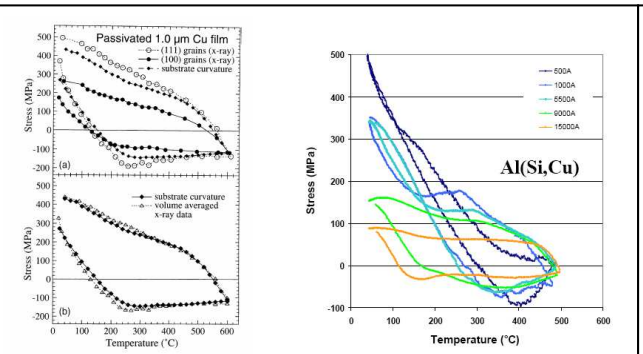


Figure 13 Non linear stress evolution during 1st thermo cycles following mayer deposit [Bostrom].

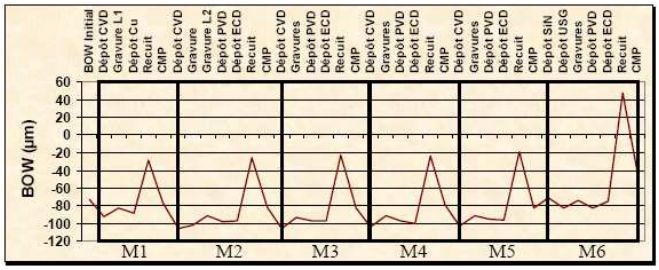


Figure 14 Typical plot of wafer warpage history during FEoL flow [Dumas].

Thermo mechanical, off balanced deposition and inelastic material response are the main stress contributors of the FEoL and BEoL process stages.

2.2 Typical stress and strain consequences

2.2.1 Specific case of FEoL strain boosters: When stress can profit to performance

To boost electrical transistor performances and following Moore's law, strain engineering is nowadays used in whole advanced technologies. Figure 15 shows ratios of performance contributors for each technological nodes, demonstrating that strain is more and more acting while devices shrink. This underlines the increasing need for the use of strain while decreasing transistor dimensions to reach performance specifications.

At a first approach, the piezo-resistive theory allows to describe physics linking strain values to resistive properties. More precisely, these proportional factors enable to roughly bond strain components with effective mobility change for both PMOS and NMOS. Qualitative effects are depicted in Figure 16: From this table, it can be read that dependence from strain to mobility is distinguished by MOS type, silicon orientation and channel direction.

Hence, to optimize performances, strain engineering will consists in playing with the relevant components, keeping in mind that effects can be either cumulated or cancelled.

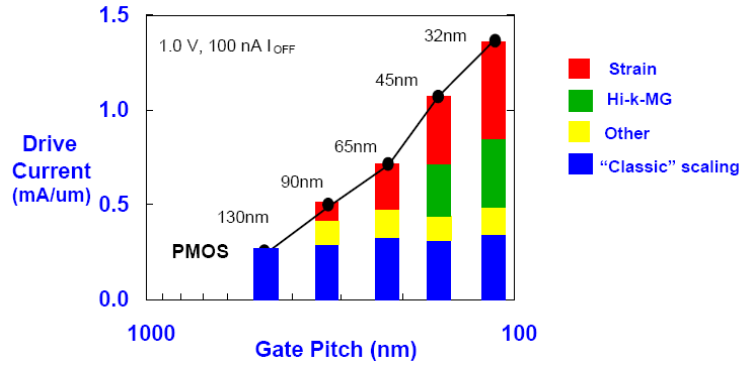


Figure 15 Transistor performance trends, strain effects. SSDM 2009.

$$\frac{1}{\rho}\begin{bmatrix}\Delta\rho_{xx}\\ \Delta\rho_{yy}\\ \Delta\rho_{zz}\\ \Delta\rho_{yz}\\ \Delta\rho_{xz}\\ \Delta\rho_{xy}\end{bmatrix} = \begin{pmatrix}\Pi_{11} & \Pi_{12} & \Pi_{12} & 0 & 0 & 0\\ \Pi_{12} & \Pi_{11} & \Pi_{12} & 0 & 0 & 0\\ \Pi_{12} & \Pi_{12} & \Pi_{11} & 0 & 0 & 0\\ 0 & 0 & 0 & \Pi_{44} & 0 & 0\\ 0 & 0 & 0 & 0 & \Pi_{44} & 0\\ 0 & 0 & 0 & 0 & 0 & \Pi_{44}\end{pmatrix}\cdot\begin{bmatrix}\sigma_{xx}\\ \sigma_{yy}\\ \sigma_{zz}\\ \sigma_{yz}\\ \sigma_{xz}\\ \sigma_{xy}\end{bmatrix}$$

Substrate		(100)		(110)	
Channel		[110]	[100]	[110]	[100]
NMOS	L	T	T	T	T
	W	T	C	C	C
	Z	C	C	T	C
PMOS	L	C	C	C	C
	W	T	-	-	-
	Z	-	-	-	-

Figure 16: Piezoresistivity matrix and mobility dependence on crystal orientation and strain: "T" means tensile is preferred, "C" means compressive is preferred and "-" means no significant effect. "L", "W" and "Z" depicts components according to transistor orientations. Engineering Shu-Lu C

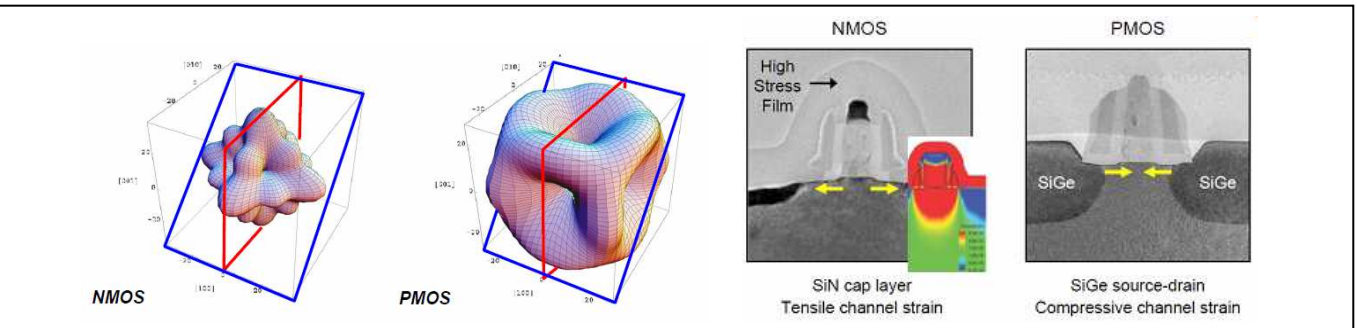


Figure 17: Mobility dependence on crystal orientation, MOS type and strain

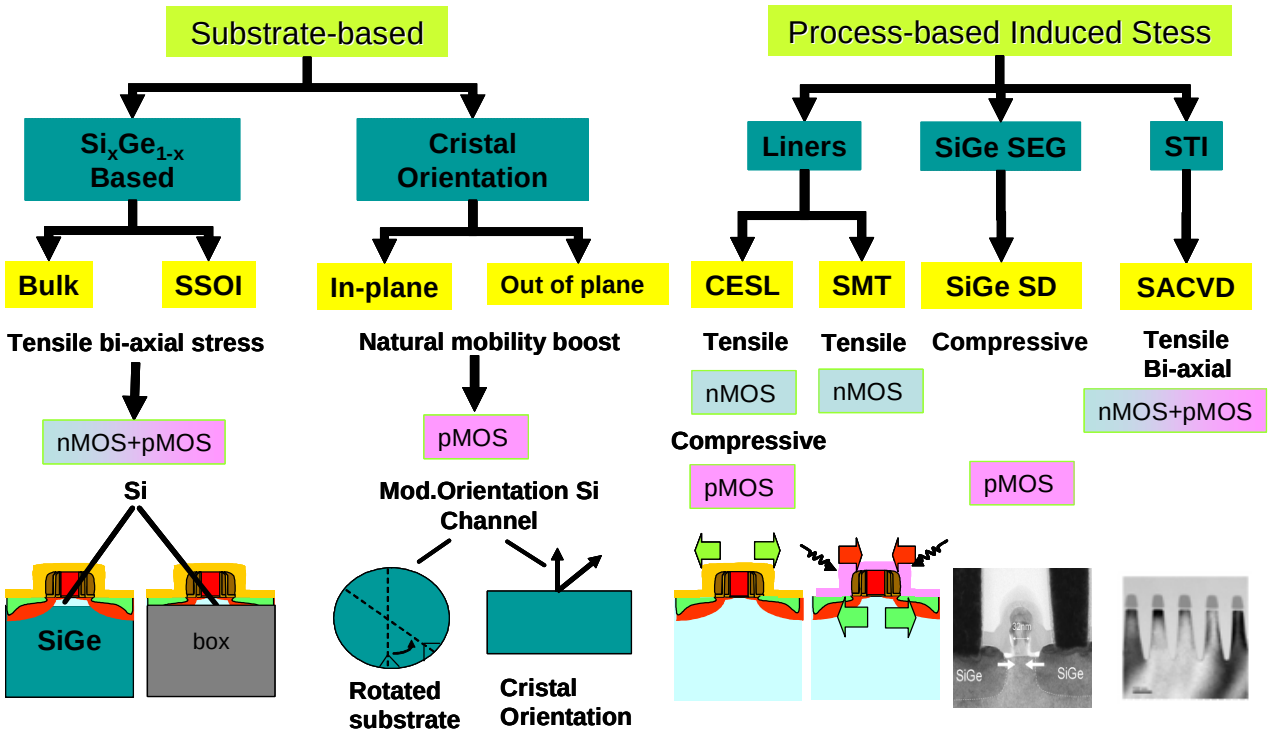


Figure 18: Schemes of Front End stressors types.[Morin]

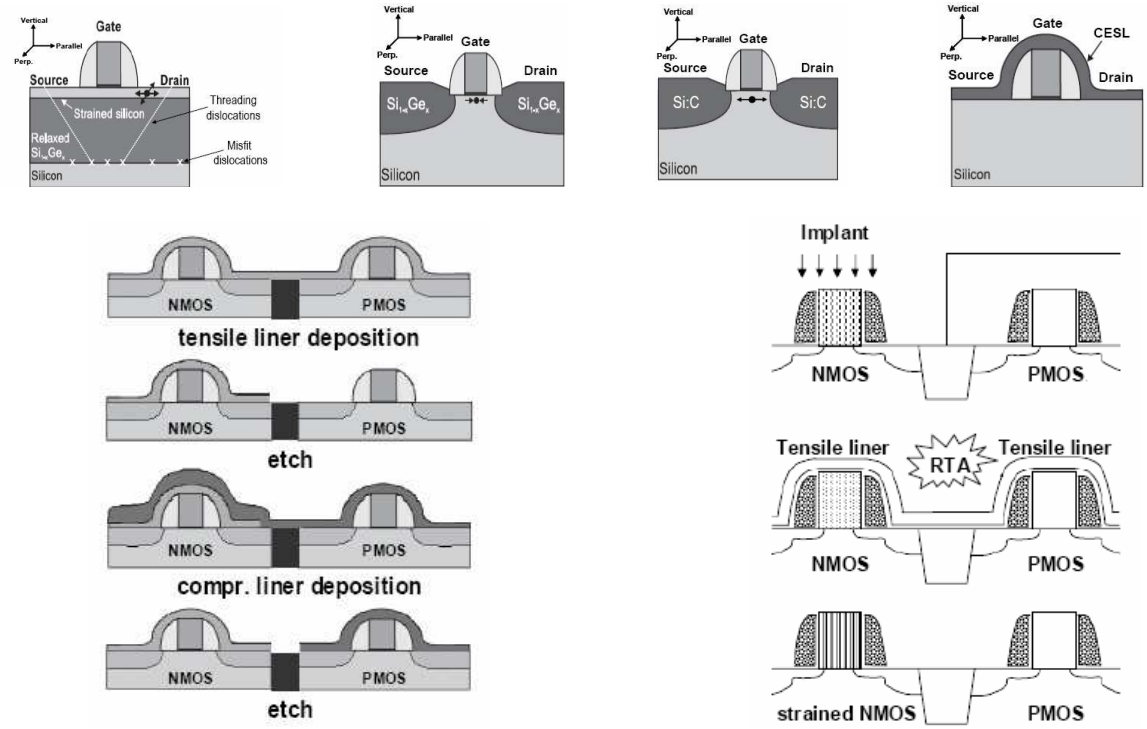


Figure 19: Front End stressors types (from left to right and top to bottom: SiGe, SiC, CESL, dual CESL, SMT [Shickova]

There are several ways to induce a strained channel, depending on the transistor type and process choice. Figure 18 and Figure 19 and shows the most commonly used schemes.

Performance improvement troughs strained channel would hence, be a smart combination of stress components. Thus, the deep understanding of stress transfer mechanisms must be achieved to allow device optimization.

2.2.2 Stress as yield loss contributor for BEoL, assembly and packaging

In the previous chapter, benefits of strained silicon for transistor performances have been briefly introduced. One modeling application will be shown later on in this thesis.

On the other hand, most of the consequences of stress are detrimental, acting on yield loss during, mostly during manufacturing and while functioning too. More precisely, stress related failures, particularly delamination and cracking in dielectrics, are nowadays determined as one of the key brake for integration.

Such fails are liable to occur at several process steps and in distinct chip regions. Many kinds of failure modes are observed, Figure 20 shows pictures and examples of typical ones at several locations inside the chip.

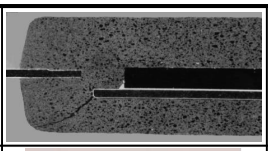
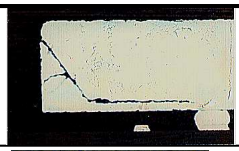
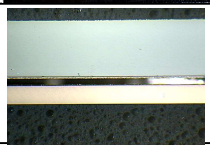
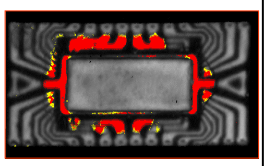
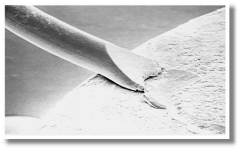
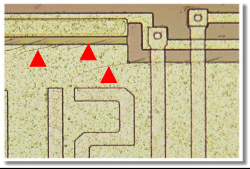
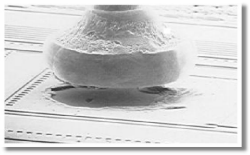
1: Package Crack		5: Die Crack	
2: Excessive Warpage		6: Die Lift	
3: Delamination		7: Stitch Break (incl downbonds)	
4: Passivation Crack / Metal Shift		8: Bond ball lift	

Figure 20 Examples of mechanical failures in IC.

Furthermore, tables in Figure 21 depict a quite comprehensive portfolio of failure mechanisms and their corresponding physics. They can be driven by a wide range of distinct causes: Complementary to the purely mechanical stress related concerns, other wet, chemical and multi physics induced fails are detected and investigated.

In the next chapters, the industrial framework to deal with thermo-mechanical cases and the needs for development of methods and optimization tools will be illustrated.

Basic failure mechanisms	#	Failure origins and driving forces	SiP-relevant failure examples	Fault isolation and failure analysis methods
A: Coherent crack formation	1	Thermomechanical mismatch	Chip solder fatigue BGA solder ball fatigue Fracture of an embedded passive component Die-to-die spacer crack Underfill crack IC metal line open	**Stress analysis** by Thermoire-Interferometry, Speckle-Interferometry (ESPI), Deformation analysis by image correlation, x-ray diffraction **Fault isolation** by Magnetic microscopy, Time domain reflectance, Lock in thermography, TIVA, OBIRCH **Crack detection** by Scanning Acoustic Microscopy, Cross section analysis with light microscopy, SEM or FIB/SEM
	2	Mechanical loading (application- or process-induced)	IC dielectric crack Organic substrate crack Solder ball crack (drop)	
	3	Hygroscopic swelling	Mold compound cracking, die cracking, substrate cracking	
	4	Reaction-induced volume shrink or expansion (e.g. curing)	Mold compound cracking, die cracking	
	5	Internal pressure (e.g. moisture vaporization at increased temperature)	Mold compound cracking, die cracking	
B: Interfacial delamination	1-5	Same as 1-5	IC dielectric delamination Underfill delamination Delamination between stacked dies Organic substrate delamination Mold compound delamination	**Stress analysis** by Thermoire-Interferometry, Speckle-Interferometry (ESPI), Deformation analysis by image correlation, x-ray diffraction **Crack detection** by Scanning Acoustic Microscopy, Cross section analysis with light microscopy or SEM, FIB/SEM, FIB/TEM
	6	Interface reactions causing loss of adhesion (e.g. moisture-, oxidation-, contamination- related)	Underfill delamination Mold compound delamination Organic substrate delamination	**Crack detection** by Scanning Acoustic Microscopy, Cross section analysis with light microscopy or SEM, FIB/SEM, FIB/TEM **Surface analysis** by TOF-SIMS, XPS, AES, TEM+EDX, TEM+EELS
C: Void and pore formation	7	Mechanical creep	IC Solder ball fatigue BGA solder ball fatigue	**Fault isolation** by Magnetic microscopy, Time domain reflectance, Lock in thermography, TIVA, OBIRCH **Void detection** by x-ray microscopy or x-ray tomography Cross section analysis with light microscopy, SEM or FIB/SEM (with EDX,WDX, EBSD and x-ray diffraction for analysis of intermetallics)
	8	Diffusion (Kirkendall void formation) and Intermetallics formation	IC UBM lift Void in IC interconnect or in via Wire bond lift BGA solder ball lift	
	9	Electromigration	Void in IC metal line or solder, Void in solder, metal line or via in the BGA substrate	
	10	Thermomigration	Void in IC metal line or solder, Void in solder, metal line or via in the BGA substrate	
D: Material decomposition and bulk reactions	11	Chemical corrosion	Bond wire lift	**Fault isolation** by Magnetic microscopy, Time domain reflectance, Lock in thermography, TIVA, OBIRCH **Failure analysis** by Cross section analysis with light microscopy or based on FIB/SEM with EDX or WDX, TEM, TOF-SIMS, XPS, FTIR spectroscopy, , mechanical testing, TGA, DMA, DSC (ageing), EBSD (grain analysis)
	12	Galvanic corrosion	Bond wire lift	
	13	Ageing (UV, …)	Organic substrate cracking or delamination Underfill cracking or delamination	
	14	Grain coarsening, phase separation	Wire bond rupture IC solder ball fatigue BGA solder ball fatigue	

Figure 21: Comprehensive table of mechanical related fails, root causes and failure analysis methods [ITRS, The next Step in Assembly and Packaging, SiP White Paper V9.0].

3 Developments of a numerical tool set for stress related topics

3.1 General objectives and requirements

Aiming to deal and manage mechanical related questions, some specific developed tools, mainly numerical, will be further depicted. Main results and added values will be underlined.

However, before giving typical examples of stress and strain engineering during technology development, the general framework and requirement for investigation tools must be presented.

The ultimate targets are to speed up and reduce costs of device integrations, by allowing un-materialized testing. These consist in setting up both experimental and numerical methods to define the touchy choice of several options during the early phases of technology developments. From the simulation point of view and as pictured in Figure 22, a permanent loop of virtual and actual tests is required to check model consistency, result relevance and model portability through technological nodes evolution.

Such whole methods, experimentally validated, are truly some significant added values for products and provide insights on technological features: Manufacturing processes, materials, recipes optimization, design rules are the main ones, and hence the proper investigation techniques are to be sought.

At the end, generic procedures would be applicable for a wide range of processes, both in the Front-End and Back End of the line.

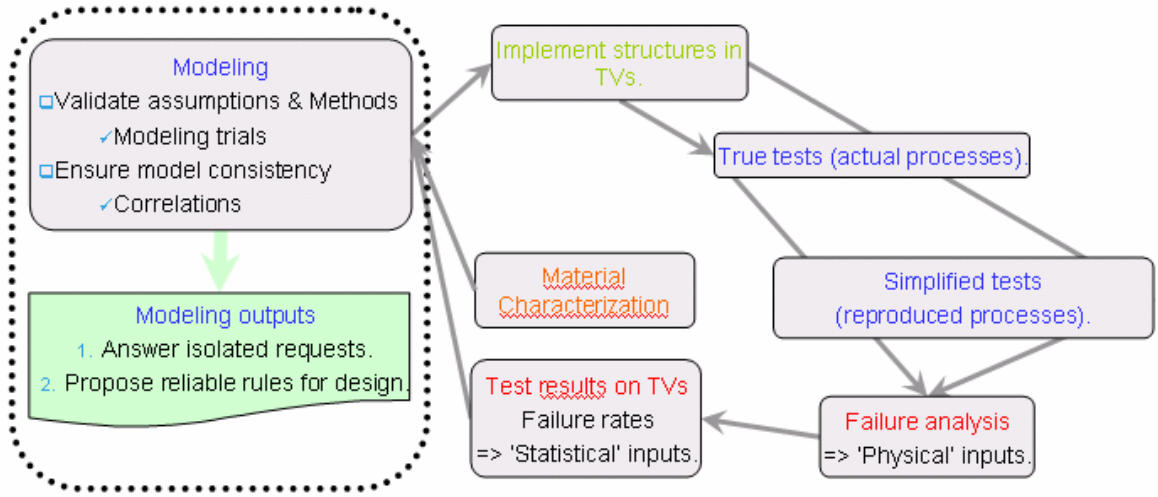


Figure 22 Schematic of requirements and targets for reliable modeling

3.2 Needs for specific developments and compromises

In the next section, a brief state of the art is done of some of the important mechanical and thermo mechanical characteristics for semiconductors devices. Despite the fact that whole of them will not be included in our models, these specific features must be kept in mind in order to determine the field of applications of the models. Hence, the relevant assumptions can be made with a clear identification of the model limitations.

3.2.1 Material properties considerations

Similarly to the critical length dimension decrease in transistor devices, the race of performance leads to reduction of the dielectric constant in isolating materials [i].

Several kinds of processes are developed to manufacture such materials. However, it is widely observed that the resistance and capacitance factor (RC) reduction are straightly correlated, thought the dielectric constant values k, to a degradation of mechanical properties of inter metal isolators [ii, p.41 1, p.41 1, p.41 4].

Indeed, since an effective way to increase the isolating ability of a material is to make it few dense. Hence, the inclusion of pores at the nanometer scale is an effective manner [iii].

By this way, one can easily guesses that such holes introduction leads to degrade the mechanical resistance [iv, v, p.41 5, p.41 5, p.41 1]. To counteract this later feature, authors propose process tricks to improve mechanical properties and adhesion features of advanced porous based dielectrics [vi]. Despite these efforts, strength of advanced interconnect stacks remains weaker compared to standard SiO_2 based ones.

As for the conductor parts of the interconnect stack, considerations on electrical properties e.g. the film ohmic resistance have promoted the adoption of copper material as replacement to the formerly used aluminum.

Besides patterning effects, the copper material itself shows quite specific behavior while deposit in thin film shapes [vii]. More precisely, the order of length between the film geometric features and the copper microstructure becomes comparable [viii]. As consequences, mechanical behavior of true interconnect structures becomes dependent to design and, targeting a complete reproduction of the stack, the actual properties of each compounding material should be set for each couple of space and width parameters [ix]. Account of the copper microstructure in each inter metal dielectric layer would hence be necessary for very deep and quantitative analysis of structures [x]. Authors publish characterization results of such patterning effects [xi]. In addition, it should be noticed that other materials used in interconnect built up show similar sensitivity to process and design effects [xii]. In

order to bridge material properties, design features and fracture mechanics, characterization results from four point bending measurements on a wide range of sample types have been reported [xiii].

Once known, we must wonder how to account the aforementioned sensitivities according to our work objectives. More precisely, the relevant sharpness level to account is not necessarily the finest one: From the modeling point of view in an industrial technology development framework, we can state that to include the whole material specificities within the full interconnect stack would not be the most efficient strategy. Indeed, on one hand it would be detrimental for analysis clarity purpose and, on the other hand, would lead to huge numerical models.

Specific assumptions and compromises will be identified and discussed in this work through application examples.

3.2.2 Mechanicals fails in Low-k/Copper interconnects

The mechanical weaknesses of materials used in advanced BEoL interconnects, underlined in the previous chapter, have an obvious detrimental impact on device reliability. More precisely, fracture related fails are more and more observed in a wide range of loading cases and process steps. Illustrations of such statement and main failure mechanisms have been published, providing a quite comprehensive overview of interconnects fails. That starts from the straightly induced stress by BEoL process and interconnect built up [xiv]. The next manufacturing steps, such as assembly processes, are also some privileged causes of delamination [xv]. The case of wire bonding induced peeling, which is chosen to illustrate our work, has been particularly studied [xv, xxv, xxiv, xxiii, xxi, xxi].

At the end, packaging process is the most representative root cause of interactions from front-end to back-end (namely FEBE compatibility concerns (FEBE), or Chip Package Interaction (CPI) fails). Many works relates parameter sensitivity studies and provide containment guidelines. Despite interactions and risk management according to package features are comprehensively reported [xiii, p.41[7], p.41 13, p.41 14], one must keep in mind that general guidelines and trends can not be totally output. Indeed, many factors remain coupled each other and dedicated studies are often required for each product or, at least, for each technology node.

3.2.3 Reliable technology development methods for FEBE interactions and assembly processes

Papers published at the time of the early phases of new dielectrics introduction have yet identified potential risk of package induced low-k fails, and proposed some methods and needed development to achieve integration of such processes [xv]. Flip-chip assemblies can be referenced as a significant illustration of failures in advanced packaging processes [xviii]. Several needs for some methodological development to deal with CPI and optimize yield loss are also suggested [xxiii].

Beyond the published papers, internal studies enabled to highlight product features and assess fracture risk. Package and die sizing, thermo-mechanical properties of underfill and molding compound are one of the effective optimization parameters.

As aforementioned and underlined, the related physics and involved scales pose a great challenge to be integrated in a day to day industrial usage. Despite the fact that the some authors report many works, no unified or standard procedure has risen. Hence, a range of tool boxes remain to be developed in order to fulfill technology evolution requirements: These concerns both experimental and numerical means. More precisely and as for the simulation frame: Optimization procedures, multi scale and homogenization models, failure and evaluation criteria must be carefully set.

Amongst the wide range of interconnect structures concerned by these fails, the so-called pad region is a privileged site. Indeed, this later must consecutively bear severe processes: Probing, then wire bonding or bumping, and finally molding steps are strong mechanical contributors. On the other hand, from a numerical point of view, several challenges must be faced to allow the understanding and the solving of such fails.

In the next part, simulation strategy and dedicated developments for interconnect structure optimization are presented.

3.3 Selected applications, numerical studies and results

In the next section, trying to draw a significant snapshot of applications; FEoL, BEoL and packaging examples are selected. The involved physics are described, and dedicated internal researches and developments are shortly presented.

Amongst the publications issued by the local STMicroelectronics team, a couple is selected as illustration purpose. Hence, to get a more detailed description of the works, the reader is suggested to refer to the following references:

- Strain engineering in FEoL:
    - *Paper "Method for managing the stress due to the strained nitride capping layer in MOS transistors, IEEE Transactions on Electron Devices, v 54, n 4, p 814-21, April 2007."*
    - *Patent «Method for managing the stress configuration in the channel of a MOS transistor, and corresponding integrated circuit » Application Number: EP20050290922 European Patent Application EP1717864 Publication Date: 2006-11-02 Filing Date: 2005-04-27*
- Fracture mechanics in interconnect BEoL:
    - Facing scale challenges with modeling: Multi levels and homogenization techniques for interconnect design.
        - *A multi scale finite element methodology to evaluate wire bond pad architectures, Thermal Mechanical and Multi-Physics Simulation and Experiments in Micro-Electronics and Micro-Systems, IEEE Cat. No. 05EX1050, p 648-55, 2005.*
    - Facing failure mode specific challenges, fracture mechanics: Energy based failure criteria for interface delamination:
        - *Gold wire bonding induced peeling in Cu/Low-k interconnects: 3D simulation and correlations. 2007 International Conference on Thermal, Mechanical and Multi-Physics Simulation Experiments in Microelectronics and Micro-Systems, IEEE Cat. No. 07EX1736, p 156-64*
    - Peeling in wire bond pads:
        - *3D multi scale modeling of wire bonding induced peeling in Cu/low-k interconnects: application of an energy based criteria and correlations with experiments. 2007 Electronic Components and Technology Conference, IEEE Cat. No. 07CH37875, p 256-63, 2007.*
    - Chip Package Interactions:
        - *Chip-package interactions: some combined package effects on copper/low-k interconnect Delaminations 2008 2nd Electronics Systemintegration Technology Conference, IEEE Cat. No. 08EX2524, p 713-18, 2008.*
        - *Advanced Reliability Modeling of Cu/low-k Interconnection in FCBGA Package. Proceedings of 56th Electronic Components and Technology Conference, IEEE Cat. No. 06CH37766, 8pp., 2006.*
        - *Multi-level numerical analysis on the reliability of Cu/low-k interconnection in FCBGA package. Proceedings of 7th Electronics Packaging Technology Conference, IEEE Cat. No.05EX1233C, p 8 pp., 2005.*

3.3.1 Strain engineering in FEoL [10, 27, 16, 18, 29, 30]

The following example shows how simulation can help to boost electrical performance thanks to CESL stressor. i.e. one of the most strained liner techniques, its integration scheme of this later is described in previous section.

According to the piezo resistive theory, the effective modification of the overall mobility depends on the combination of the whole stress components. The aim of the modeling is here to evaluate separately stress components and to depict device layout dependence. This allows to output comprehensive design and process rules and to forecast transistor features.

Three dimensional models, with parameterized geometry are used. Thanks to symmetry, a quarter of a device is simulated as shown in Figure 23, and the resulting stress components are plot in Figure 24 as a function of the channel length.

Strain relaxation phenomena are induced from a capping strained layer. Indeed, according to process conditions, one can deposit such film, which have residual stress at ambient temperature both due to CTE mismatch and intrinsic constrains.

Hereafter the main outputs from simulation, these are described in more details in our publications.

More precisely, 3D CESL simulation shows channel stress features as a function of the device architecture. The stress averaged along the channel length, locally induced, behaves as follows:

- Along channel length direction, a tensile stress is observed in any cases.
- The lower the channel length (noted L), the higher the stress. "Edge" effects are in these case dominant, contrary to "full sheet" effects.
- A tensile residual transverse stress is observed only for short values of L and W. On the opposite, for large L and W, transversal stress becomes compressive. This underlines that "central effects" are dominant.
- Finally, a vertical compressive stress is generated too. This later is induced by the gate walls and value also depends on the in plane geometry of device.

As a conclusion, by analogy with springs mounted either in parallel or in serial, both direct and indirect effects are determined by simulation. Furthermore, Figure 26 shows edge vs. central stresses according to the device geometrical features.

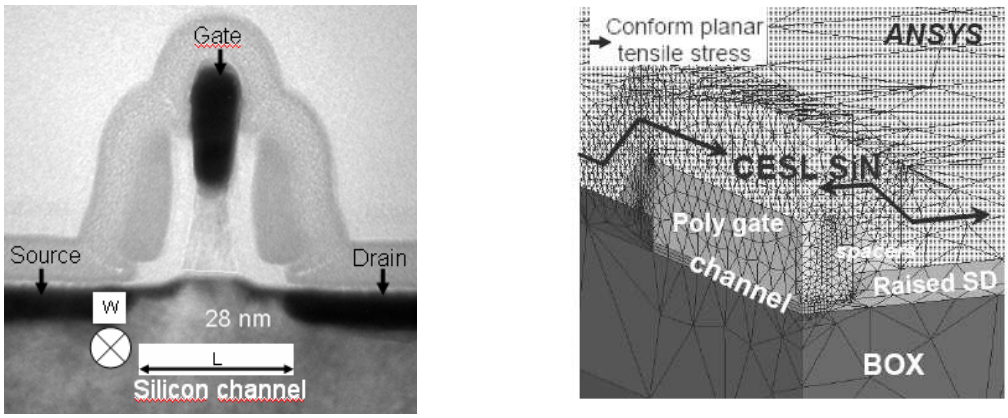


Figure 23 Transistor X-Section and Finite element model for CESL induced strain simulation

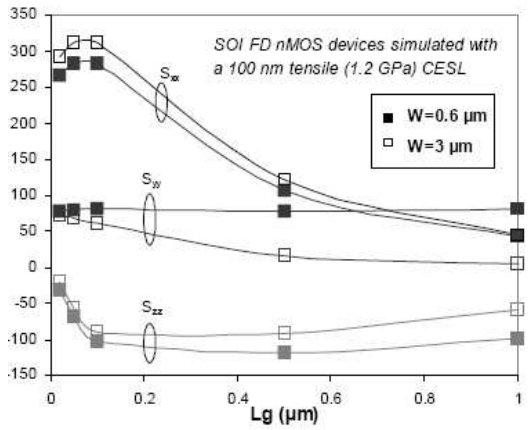


Figure 24 Channel stress averaged [MPa], of the three orientation normals, as a function of gate length and for 2 gate width values.

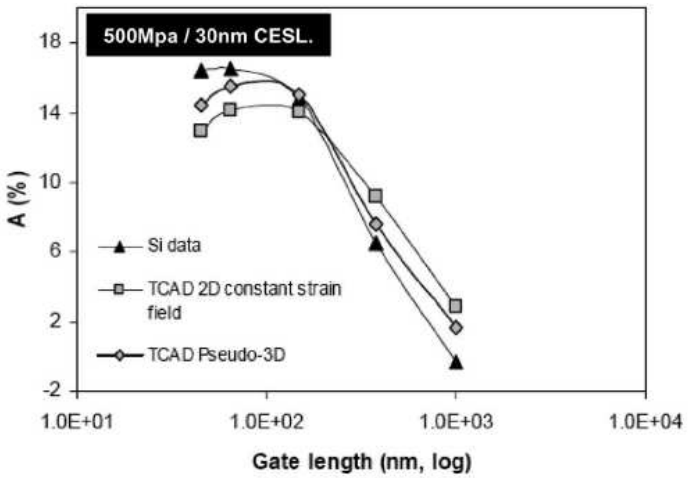


Figure 25 Comparison of the simulated saturation current enhancement ratio to the experimental data as a function of the gate length.

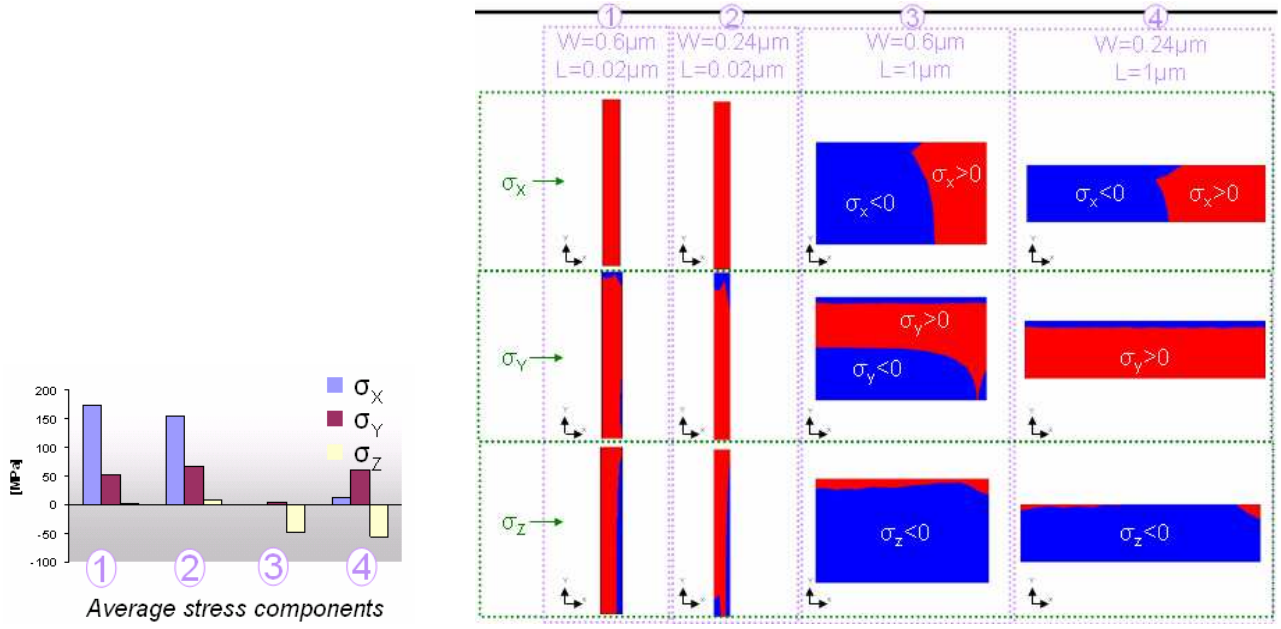


Figure 26 Channel stress dependence for distinct device architectures. The leftmost area of the figures corresponds to the channel center (i.e. symmetry plane). Tensile and compressive stress are respectively shown with red and blue colors.

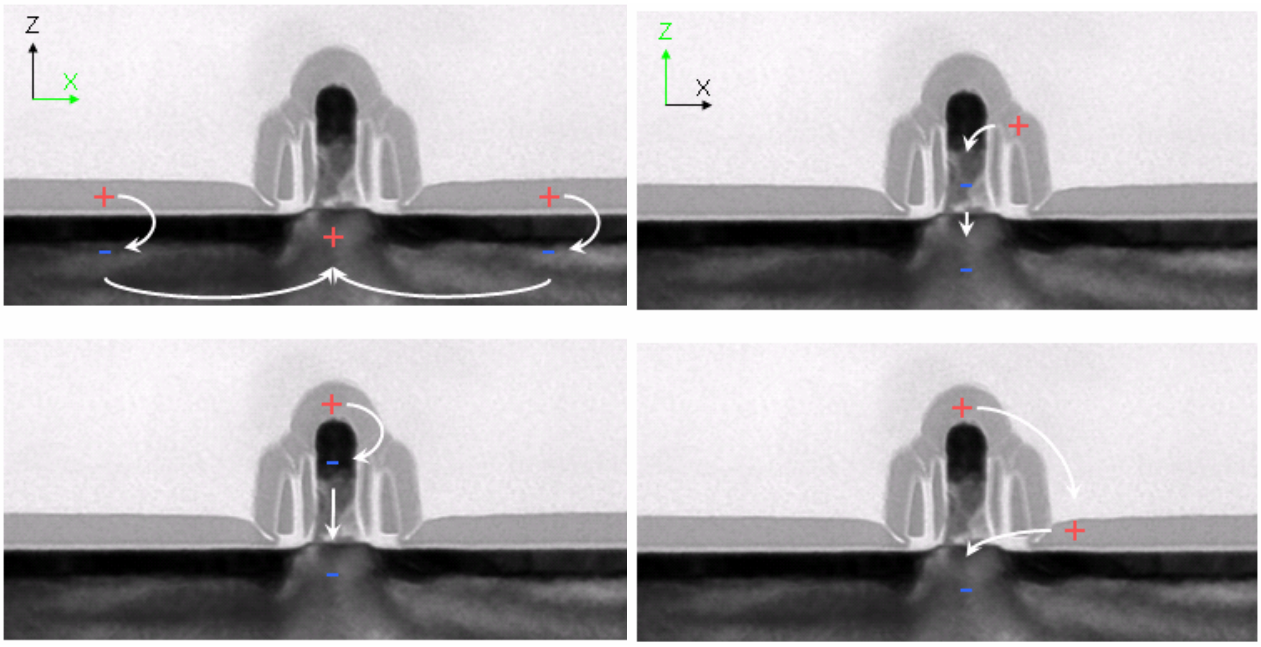


Figure 27 Pictorial description of stress transfer mechanisms from the strained layer to the channel.

Further to this analysis and using the previously described piezo resistive coefficients (p. 12), electrical performance boosting can be output.

On the other hand, it should be noticed that strain engineering could reach some limitations. More precisely, it is obvious that stress can not be input up to infinite values: Defect nucleation, dislocation generations or micro structural changes would lead to performance decrease, such as electrical leakage, opens or shorts, and finally could question device integrity.

As a conclusion for the strain engineering folder, this is obvious that simulation can be an essential tool for technology development. Indeed, numerical modeling is the only way to provide comprehensive investigations of the FEoL process induced strain in silicon, and thus bridge the piezoresistive related physics. More precisely, the main added values provided by this thesis range from a "with hand" understanding of stress transfer mechanisms, predictive mechanical simulation to calibrated models from device layout to electrical mobility.

3.3.2 Fracture mechanics in interconnect BEoL

As previously introduced, most of the consequences of the stress is detrimental and leads to yield decrease. Furthermore, pursuing the race for miniaturization and electrical performance, the interconnect BEoL regions are known to be preferential sites for mechanical issues.

3.3.2.1 Facing scale challenges with modeling: Multi levels and homogenization techniques for interconnect design [19].

The dimension range from the transistor scale to the chip, i.e. several decades of difference, must be accounted for. Indeed, macroscopic loads, such as packaging ones, induce fails within the silicon and interconnect. For modeling purpose, this later difficulties must be faced according to computer limits. Example of wire bonding concerns, which remains the main used assembly process, is presented:

The bond pad has a connecting function; it links the die and the package and consequently assumes the functionality of the entire chip. First of all, it must resist to compressive stress and ultrasonic vibrations during the wire bonding and afterwards to tensile and shear stresses during the qualification procedures. The reliability of the bond pads has become a major concern with the introduction of new dielectrics and with the continuous downscaling of the pad size. Experimental results highlight that failures occur either by peeling of the interconnection levels, cratering deep into the silicon, or non-sticking between the top metal layer and the wire. Mechanical simulations will investigate the first failure mode.

Typical dimensions of the domain of interest have a very wide range: During the wire bonding process, macroscopic loads are involved by the wire, with dimensions about 40µm corresponding to the ball diameter. On the other hand, the interconnect levels, where the location of the failures investigated here are located, are composed by very thin layers. Submicron patterns compound these layers. Moreover, the choice of a three dimensional analysis should be preferred to a commonly used plane strain assumption. Thus, to consider this very detrimental aspect ratio would lead to a huge amount of elements with a single FE run. Multi-level modeling needs to be performed.

The main steps of multi level modeling are the following: - Compute a first simulation at global level to get displacements field. - Locate the maximum strained area, i.e. the future location of the micro model. - Apply the displacement field calculated at the macro level as boundary conditions of the micro model in order to reach the local stress field.

This approach can be used either linearly (i.e. a single set is ran and no loop between stress results obtained locally and globally is carried out), or non linearly: The later option allow to account strong coupling effects, however it obviously increases the total simulation time. The linear approach is chosen here, with respect to our objectives and the suspected magnitude of the aforementioned non linear phenomena.

One of the key points here is to be able to describe the materials and the layout which composes the macro model with a sufficient amount of details in order to calculate properly the displacement field. At this stage, a homogenization procedure needs to be carried out. This enables to take into account the geometrical details by modifying the mechanical properties, without meshing all the bond pad layers. There are several ways of doing the homogenization step, and the most suitable depends on the model details, i.e. the geometrical features, materials and also the loading cases. Since pad structures are usually periodically designed, a representative unit cell (RUC) can be chosen and finite element models must be built respectively. The equivalent mechanical behaviors of each RUC are computed thanks to basics loading cases (i.e. pure tensile, shear and uniform thermal ramp) Figure 31.

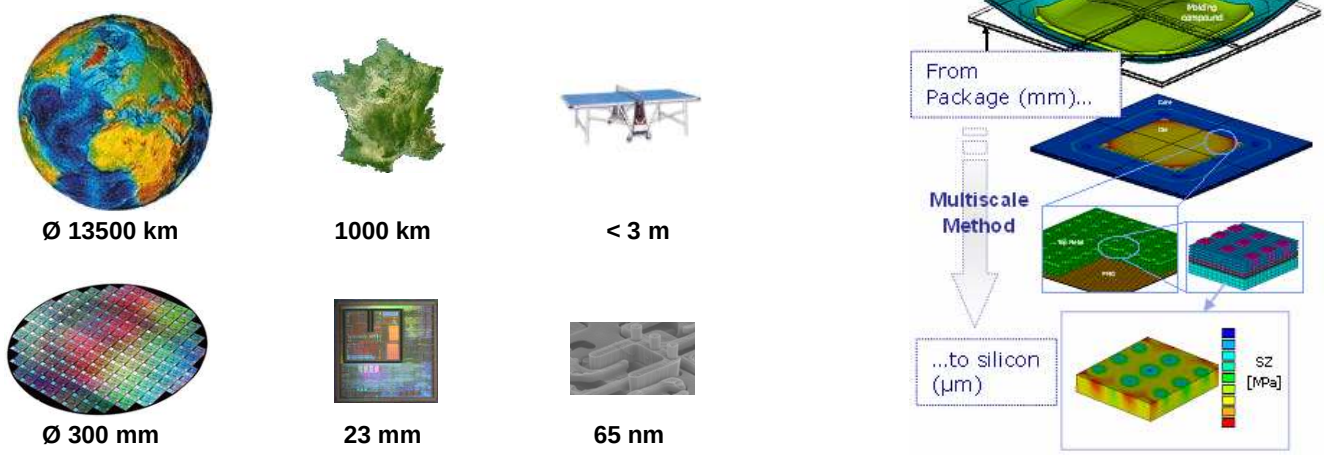


Figure 28 Dimensional analogy (left) and multi level modeling example (right).

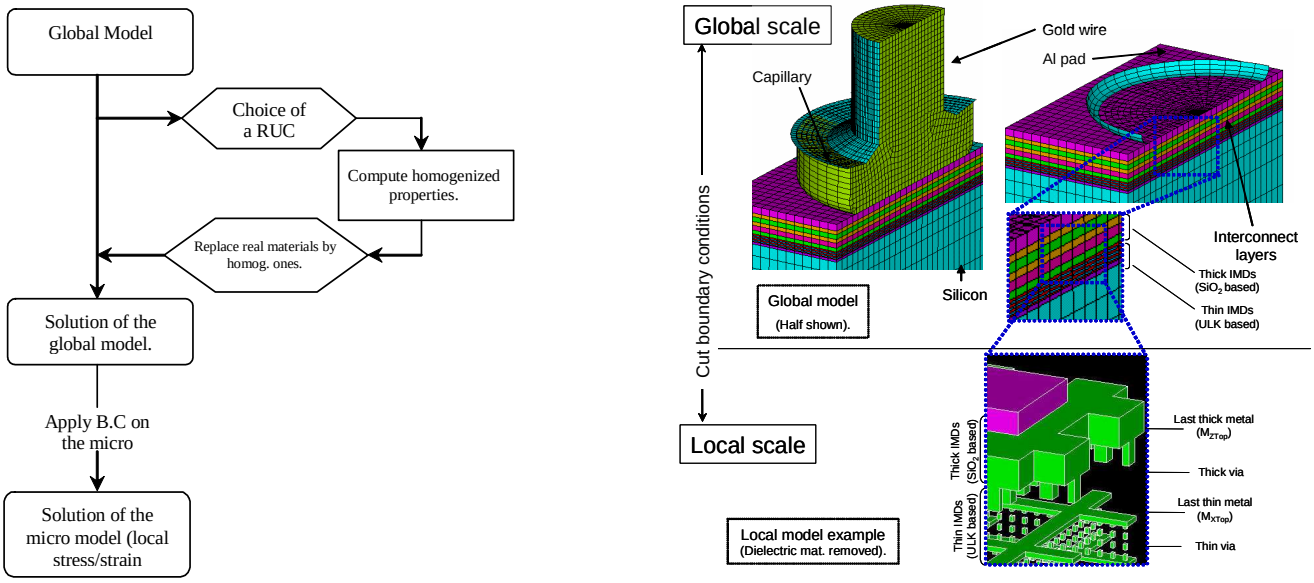


Figure 29 Multi Level and homogenization technique flow chart (left), application example (right).

Modeling of the inner pad	Geometrical details	Material properties	CPU usage
Reference	Yes	• Isotropic • 1 per material	☹
Homog. I	No	• Orthotropic • 1 for all layers	☺
Homog. II	Partial	• Orthotropic • 1 per layer	😐

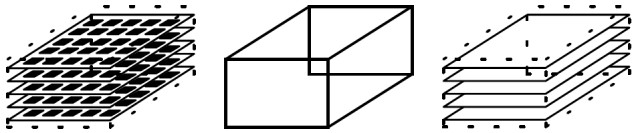
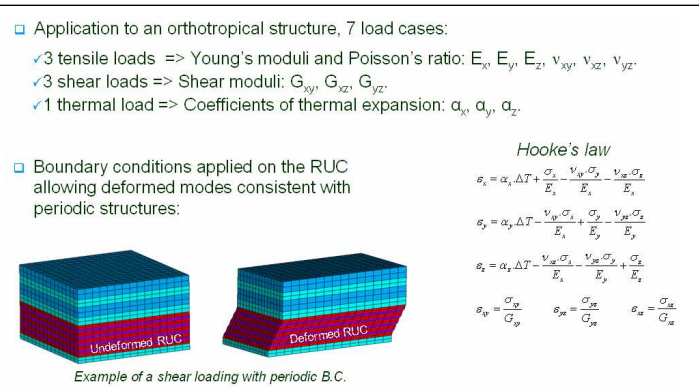


Figure 30 Comparative table and schematics of the 3 tested homogenization techniques (Reference case with a full details discretization; Homog. I with 1 orthotropic material for all the layers; Homog. II with 1 orthotropic material per layer).



#	Thicknesses [µm]	Ex [GPa]	Ey [GPa]	Gxy [GPa]	αx [.-6.^-1]	αy [.-6.^-1]	νXY
Pad	1.45	71.24	70.42	26.24	22.71	23.42	0.34
M7	0.85	82.87	127.81	29.53	9.67	13.01	0.27
V6	0.6	68.50	72.45	23.62	5.37	8.55	0.27
M6	0.85	82.87	127.81	29.53	9.67	13.01	0.27
V5	0.6	61.90	71.19	23.10	5.48	8.70	0.26
M5	0.14	17.48	127.12	7.40	15.18	15.30	0.06
V4	0.12	25.99	27.39	5.12	7.61	11.77	0.11
M4	0.14	17.48	127.12	7.40	15.18	15.30	0.06
V3	0.12	25.99	27.39	5.12	7.61	11.77	0.11
M3	0.14	17.48	127.12	7.40	15.18	15.30	0.06
V2	0.12	25.99	27.39	5.12	7.61	11.77	0.11
M2	0.14	17.48	127.12	7.40	15.18	15.30	0.06
V1	0.12	25.99	27.39	5.12	7.61	11.77	0.11
M1	0.13	43.46	126.60	8.98	11.36	14.56	0.12
PMD	0.3	60.0	60.0	24.0	2.7	2.7	0.25

Figure 31 Scheme of computation of equivalent mechanical properties of a Representative Unit Cell (left). Output parameters example (right).

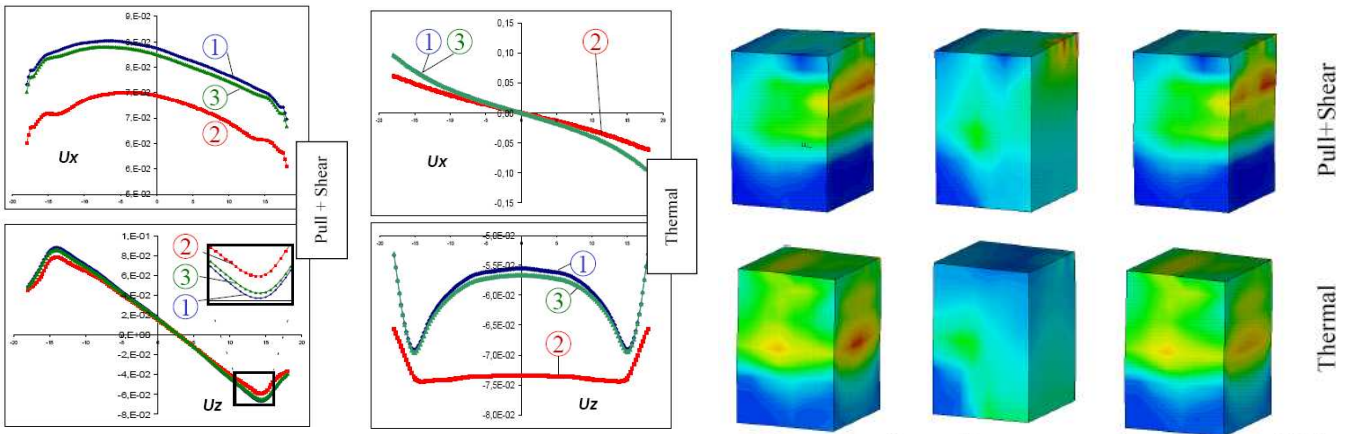


Figure 32 Left: Tangential (Ux) and normal (Uz) displacements for the 3 approaches (1: reference, 2: Homog.I, 3: Homog.II) andfor pull+shear loading and thermal loading. Right: Von Mises equivalent stress field calculated from the 3 approaches at the local scale (Reference case, Homog.I, Homog.II) and 2 loadings (Pull+Shear, thermal).

Hence, targeting interconnect optimization, it has been shown that a layer by layer homogenization is the most efficient strategy. Indeed, results comparison both in term of displacements at the global scale and stress fields at the local one, underline that an undersized discretization in the macro model will not be able to capture true stress values and locations at the micro scale.

As a result, for a reliable optimization of interconnect structures, one representative unit cell per each inter-metal layer must be chosen. It leads, for a typical stack in 65nm technology, of about a dozen set of parameters, i.e. more than a thousand of distinct mechanical properties for the whole die BEoL.

3.3.2.2 Facing failure mode specific challenges, fracture mechanics: Energy based failure criteria for interface delamination [14]

Once the finite element model and its loading conditions defined, the most suitable manner to analyze the FE results remains tricky. It must be carefully selected, according to the failure mechanisms and according to the objective of the simulation. Indeed, to relevant post processing method is a compromise between accuracy, implementation easiness, and CPU features. In that frame, an energy based failure criteria has been developed and proposed. This is derived from the Griffith theory and, despite few limitations, its added values compared to stress based one is proven, particularly for structure discrimination and interconnect design optimization.

The so-called Nodal Released Energy (NRE) post processing procedure is based on the computation of energetic quantity from the nodal solution. To evaluate the NRE value at each node, two simulations are required: One with an undamaged model, the other with the damaged one, where a virtual crack has been inserted. At this step the crack properties need to be defined by the analyst. Location, dimension and orientation of the suspected damage is chosen thanks to a preliminary analysis of the stress values. It is then possible to compute NRE values for all nodes and thus to get complete data. But this later option could be CPU time consuming in the case of large models. Figure 33 shows the post processing flow chart and formula. However, attention must be paid on the numerical parameters to be used. The sensitivity and the gap from the NRE quantity compared with the true energy release rate defined in the Griffith's theory is a manner of fact.

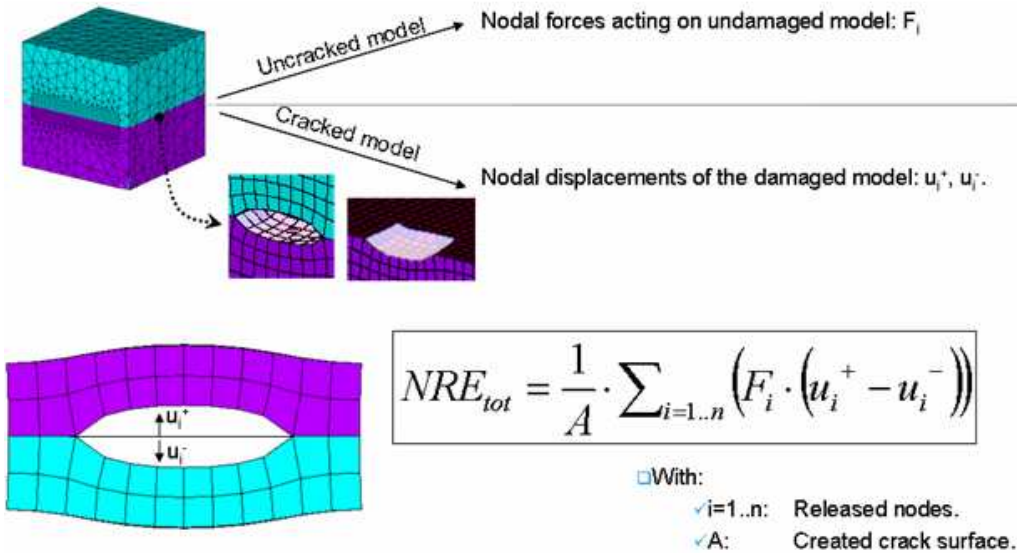


Figure 33 Energy based failure criteria: Nodal Release Energy (NRE), flow chart and formula.

3.3.2.3 Applications: Simulations and correlations

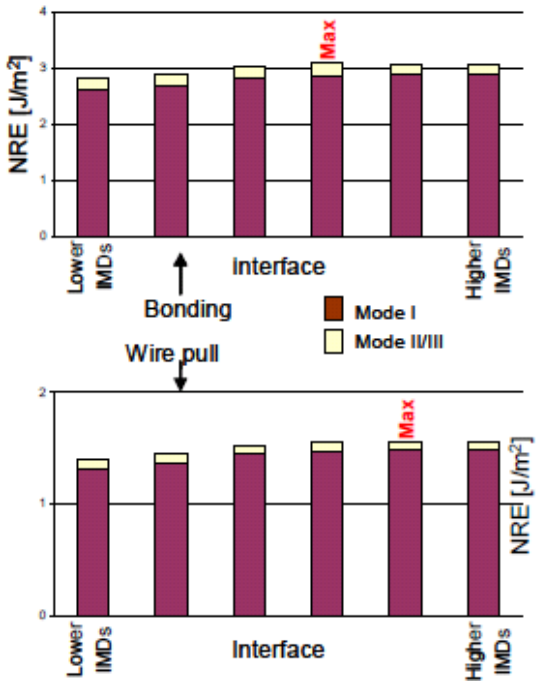
In the previous chapters, specific modeling methodologies to address Back End devices optimization have been depicted. In the followings, some results on dedicated applications are highlighted. Focuses are put on the added values of the aforementioned numerical methods.

More precisely, the insights in terms of designs comparison and fracture predictions provided by the energy based failure criteria are underlined. Indeed, contrary to a standard stress based analysis, the Nodal Release Energy proves complementary abilities in:

- Forecasting accurately the failed location in the interconnect regions.
- Discriminating designs of structures, and hence allowing interconnect optimizations.
- Guessing cracking threshold, and by consequence providing more quantitative inputs on fails.

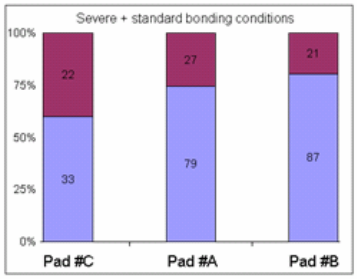
3.3.3 Peeling in wire bond pads [11]

In this section, several insights according to wire bonding fails are provided by modeling. These concern peeling failures in advanced interconnect stacks which have been observed during early process optimization of 65nm technology node. On the behalf of these processes optimization, numerical predictions have been faced to actual failure analysis and good agreement has been found, granting methods for prediction and technology development purposes.



Load →	Bonding		Pull test	
Architecture type →	Donut	From donut to line	Donut	From donut to line
Stress based analysis				
Max peeling [MPa]	41.5	+1%	87.6	+1%
Max comp. [MPa]	-142.5	0%	-32	+2%
Max VM [MPa]	129	-0%	80.9	+1%
Energy based analysis				
NRE_{TOT}	0.768	+8%	1.09	+6%
NRE_1	0.699	+6%	1.03	+5%

Figure 34 Some added values of energy based failure criteria for fracture location and design evaluation: Left: Failed interface in interconnect predicted by NRE. Right: Structure discrimination from stress based and energy based criteria.



Pad #	Local model (copper mat. only)	Pattern size	Metal layout type	Experimental ranking	Modeling ranking
D		Wide	Donuts	Not tested	Best
B		Narrow	Donuts	Best	Intermediate +
A		Wide	Lines	Intermediate	Intermediate -
C		Narrow	Lines	Worst	Worst

Figure 35 Experimental vs. numerical results: Beyond good agreement and correlations, simulation allows virtual evaluation of untested structures.

As a summary of the findings, it can be underlined that:

- Delaminations are not located at the top interconnect interfaces, which should be expected since this region is the most stresses one. In fact, fractures are observed in the quite middle of the low-k layers, as confirmed by the evaluation of the released energy (Figure 34, left).
- Figure 34 right, shows added values of the NRE compared to stress based analyze. Indeed, applying the second criteria, both location and pad discrimination is not possible.
- Four distinct pads were designed, but only three were possible to be tested. Modeling shows good agreement on the tested pad behaviors, and forecasts resistance for the untested one. This was particularly useful since the untested design was found to be the straightest one as shown in Figure 35, hence enriching design rules.

The whole frame of this work is described in the paper afore referenced. Besides, quite a wide range of modeling experiments has been preliminary carried out in order to point out and tune simulation parameters (e.g. friction condition, material approach, loadings, etc.).

3.3.4 Chip Package Interactions [3, 4, 8, 14, 15]

The second example of BEoL optimization is related on chip-package interactions, in other words, focus is put on fails located in interconnect (FE) regions which occur during packaging steps (BE). These are also named FEBE interactions or die to package compatibility concerns. More precisely, despite the fact that mechanical integrity of the die remains safe during FEoL integration, loadings during the next process steps lead to interconnection fails. Solving this kind of issue could be achieved with both FE and BE parameter tuning, since the fail is a combination of many factors. The first hardness to solve the concern is off course to identify the most relevant couple, considering efficiency, cost of integration, time for validation, etc. For that reason, this is clear that virtual prototyping is a powerful tool.

Two distinct studies are presented: The first one aims as showing the agreement of the package simulation on deformation measurements, giving confidence in the model.

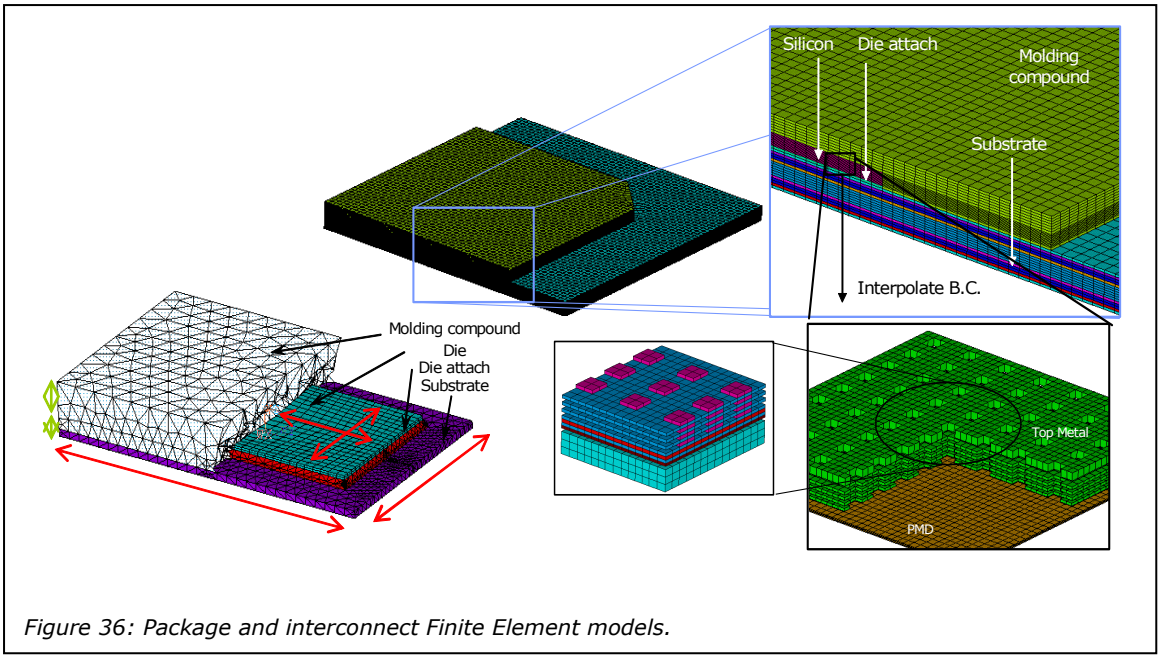
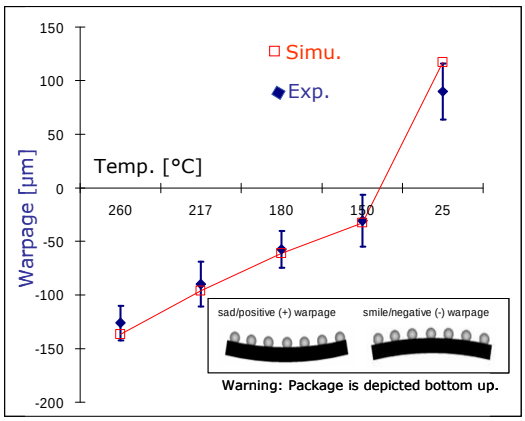


Figure 36: Package and interconnect Finite Element models.



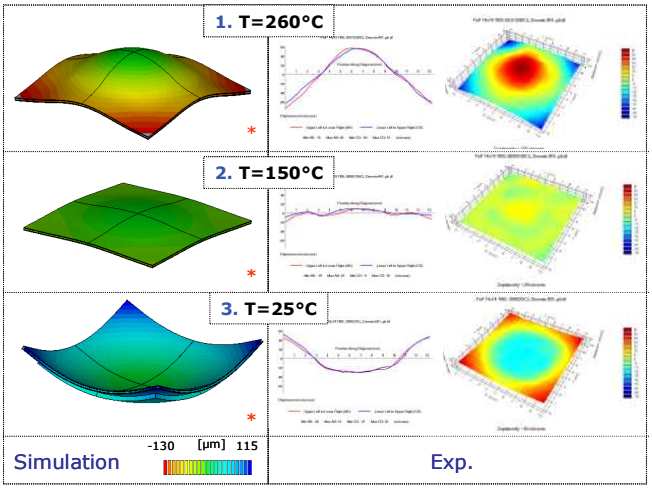


Figure 37: Comparison between experimental and simulated package corner displacements at distinct temperatures. Comparison between measured (right) and simulated (left) package displacements figures at 260°C (top), 150°C (middle) and ambient temperatures (bottom).

Indeed, simulation of the package is performed and warpage map is output. It must be noticed that modeling results in Figure 37 have been obtained by the fit of a single parameter, which is the

temperature value for a flat package. Displacements are then calculated at several temperatures, giving confidence, thanks to comparison with experimental fields, in the whole model reliability.

The other study is a more prospective work on fracture hazard in interconnects, based on numerical investigations. This one was initiated by the need for prototyping at the early stage of product introduction and potential risk assessment. Excepted on warpage measurements, dedicated correlations are not carried out here, particularly on fracture mechanics.

Again, the whole modeling strategy is described in more details in references, and only main results are depicted in the next paragraph, revealing such innovative insights in term of interconnect designs.

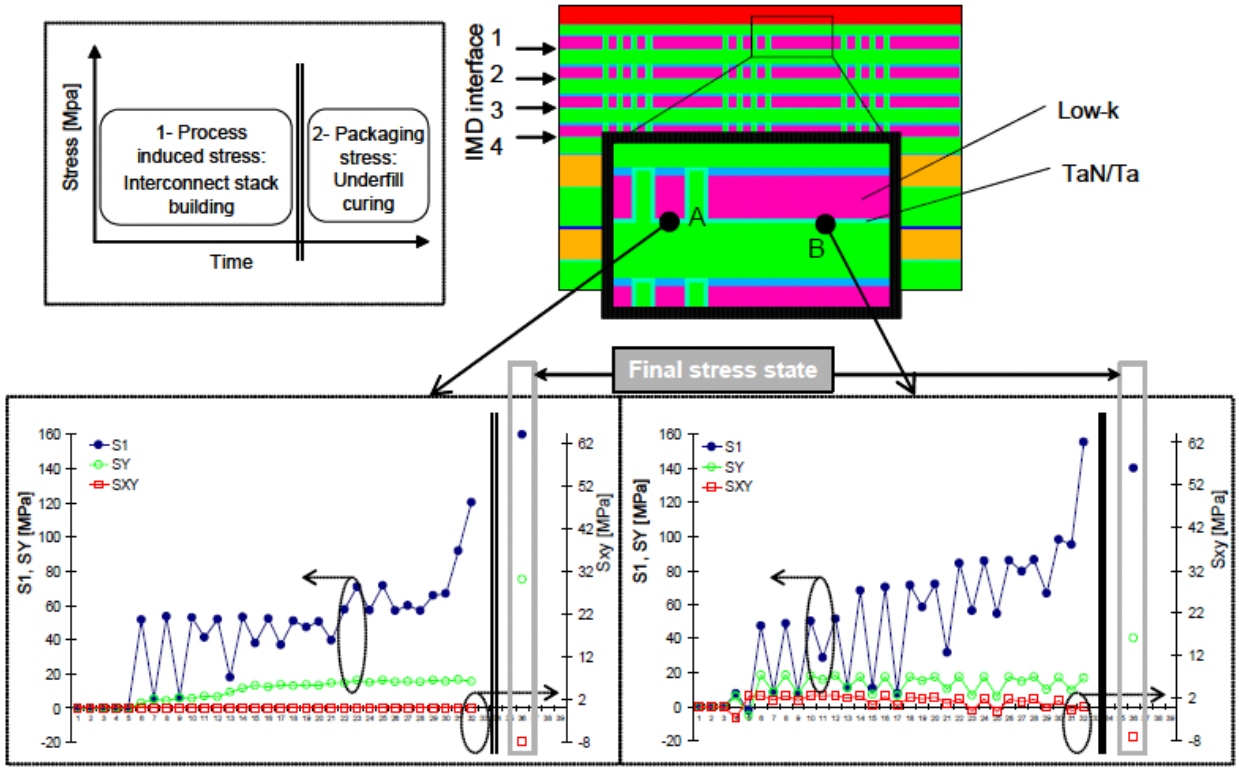


Figure 38 Full stress history evaluation, from interconnect built up to packaging allows to determine critical process steps.

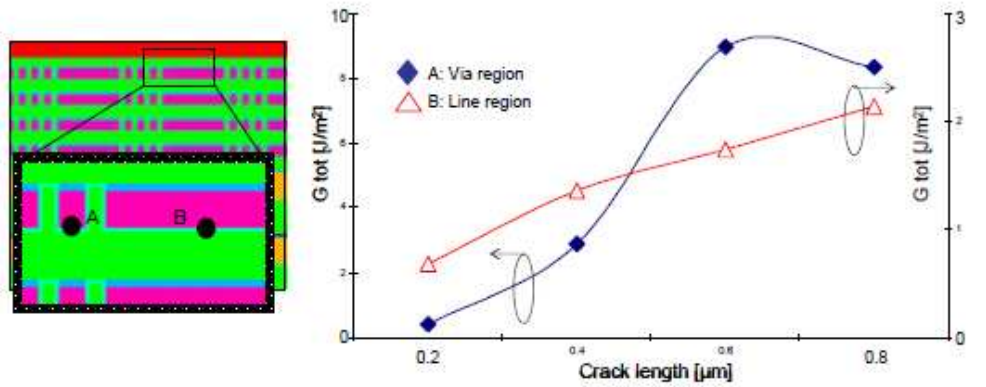


Figure 39 Cracking hazard dependence according to local patterning and critical crack length.

Concerning the modeling strategy, the process history is considered, and the final stress and strain fields are hence evaluated as an addition of interconnect build up and package stresses. Once calculated the stress state of the interconnects, the NRE method is then employed to assess fracture hazard at several locations; aiming to draw a crack behavior with respect to patterning. More precisely,

several locations are tested with variable crack length. From the evolution of the energy values as a function of the delamination length, a non monotone shape is found in region where metal patterning is narrow. Assumption could be made that such drop of the released energy is usable to tune architecture characteristics.

As a conclusion for that second example related to FEBE interactions, hereafter some of its key points:

- a full simulation of the process steps is conducted, allowing to track stress history in low-k stacks, and hence to determine the precise step where fracture can be expected (Figure 38).
- A general stress increase during interconnect built up has been found. On the other hand, stress variation has been pointed to depend on local layout, particularly at the final molding steps (Figure 38, bottom).
- Investigation on typical line and via regions brings additional design inputs. It was particularly observed a drop in the released energy values for specific patterns (Figure 39).

Further to this work, delamination hazard according to stack features, metal patterning and dependence to technology nodes and materials was started. Drawings for general rules and guidelines were initiated.

4 Conclusion

The work reported here aims to provide to the reader some features on several items related to the microelectronic industry. The content is built in order to, even for non expert of the semiconductor fields, allow a comprehensive understanding of the technology development problematic. Its range from general considerations, to applications and researches on mechanical challenges. These later have been investigated in the last few years within STMicroelectronics.

Hence, starting from a general description of the microelectronic device market, the main processes of chip manufacturing are depicted. Then, focus is put on mechanical and thermo mechanical phenomena occurring during manufacturing and qualification tests. Challenges of such mechanisms are presented, and the need for a deep understanding of the physics is highlighted.

Requirements for numerical tools, and the industrial context, are justified underlining the need for smart compromises.

Specific numerical methods have been developed, implemented and tested. Results have been faced to experimental results for correlation purposes, allowing additional insights and virtual prototyping.

This work proposes, trough a selection of applications, to briefly show results on FEoL, BEoL and packaging features of the device. Extracted from team publications, typical examples of strain engineering and fracture mechanics investigations are presented. Their added values are highlighted.

This thesis would help people to get familiar with some methods to deal on mechanical and thermo mechanical topics in a technology development framework of the microelectronic industry.

5 Appendixes

5.1 List of publications and patents

5.1.1 Publications

Conferences with Proceedings and Referees

1. Gallois-Garreignot, S.; **Fiori, V.;** Nelias, D.
   Package induced low-k delaminations: Numerical developments and experimental investigations to address FEBE compatibility fracture phenomena
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   Chip-package interactions: some investigations on copper/low-k interconnect delaminations
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4. **Fiori, V.;** Gallois-Garreignot, S.; Tavernier, C.; Jaouen, H.; Juge, A.
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   2007 International Conference on Thermal, Mechanical and Multi-Physics Simulation Experiments in Microelectronics and Micro-Systems, IEEE Cat. No. 07EX1736, p 115-21. *
8. **Fiori, V.;** Lau Teck Beng; Downey, S.; Gallois-Garreignot, S.; Orain, S.
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9. **Fiori, V.;** Verrier, S.; Orain, S.; Girault, V.
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    Ultra-thin fully depleted SOI devices with thin BOX, ground plane and strained liner

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13. Brillet, H.; Orain, S.; **Fiori, V.;** Dupeux, M.; Braccini, M.
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21. Cacho F., **Fiori V.**
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5.1.2 Patents

1 GIRAUDIN Jean-Christophe, **FIORI Vincent**, DELPECH Philippe.
« Circuit intégré comprenant au moins un condensateur et procédé de formation de condensateur ».
Publication number : FR2885452
Filling date : 2006-11-10
2 **FIORI Vincent**, ORAIN Stéphane, ORTOLAND Claude.
« Méthode pour gérer la configuration du stress dans le canal d'un transistor MOS et circuit intégré correspondant »

Publication number : EP1717864
Filling date : 2006-11-02

3 GIRAUDIN Jean-Christophe, **FIORI Vincent**, DELPECH Philippe.
«Integrated circuit having at least a capacitor and manufacturing method of the capacitor ».
European Patent Application: EP1720198 / EP20060290681
Filling date : 2006-11-08

4 **FIORI Vincent**, ORAIN Stéphane, ORTOLAND Claude
«Method for managing the stress configuration in the channel of a MOS transistor, and corresponding integrated circuit »
Application Number: EP20050290922 European Patent Application EP1717864
Publication Date: 2006-11-02
Filing Date: 2005-04-27

5 GIRAUDIN Jean-Christophe, **FIORI Vincent**, DELPECH Philippe
«Integrated circuit comprising at least one capacitor and process for forming the capacitor »
Application Number US20060255427 11/415393
Publication Date: 20061116
Filing Date: 2006-05-01

6 FIORI Vincent, GALLOIS-GARREIGNOT Sebastien, DELPECH Philippe
« Structure de protection peripherique anti-delaminage de la partie superieure d'une puce de circuit intégré »
Application Number: FR N°09/53999
Filing Date: 2009-06-16

7 KERMARREC Olivier, **FIORI Vincent**
«Metals layout for limited defects or stress propagation in ICS» "Couche métallique de protection structurelle d'un circuit intégré"
Application number: 0955936 100005979
Filing date 31 août 2009-08-31

8 **FIORI Vincent,** HOTELIER Nicolas, PRUVOST Julien, DELOFFRE Emilie
"Plaquette comprenant des puces electroniques permettant une decoupe amelioree" / "A wafer comprising electronic chips adapted to an improved sawing"
Application number: 10/50822 - 09-GR3-265 / B9978
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2 International Technology Roadmaps 2007 redaction committee: http://www.itrs.net/Links/2007ITRS/Home2007.htm

3 International Technology Roadmaps 2009 redaction committee: http://www.itrs.net/Links/2009ITRS/Home2009.htm . Or in Future Fab Issue 32 http://www.future-fab.com/download.asp

4 Invited talk to CNRS workshop: http://www.im2np.fr/GDR-Mecano/ecolenano-objets2010/index.html

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5.3 Selected publications

5.3.1 A Multi Scale Finite Element Methodology to Evaluate Wire Bond Pad Architectures.

V. FIORI [(1)], S. ORAIN[(2)],
(1) STMicroelectronics, 850, rue jean Monnet. F-38926 Crolles Cedex (2) PHILIPS semiconductors, a division of Philips France. 850, rue jean Monnet. 38926 Crolles cedex.

5.3.1.1 Abstract

This work focuses on a multi scale Finite Element Method (FEM) in order to model the wire bonding process. The methodology and results aiming at understanding and predicting the bond pad failures are detailed. Due to the very detrimental aspect ratios involve in the wire bonding process modeling, the use of a multi-level technique is mandatory. However, results highlight that precautions are needed at the macro scale when choosing the Representative Unit Cell (RUC) during the homogenization step. More precisely, a simple law of mixture leads to a wrong evaluation of the displacements at the global scale and impacts strongly the local stress field.

The FE method is applied in a linear three dimensional analysis. Both thermal and force loadings are tested and their contributions are discussed on several wire bond pad layouts.

5.3.1.2 Introduction

The bond pad has a connecting function, it links the die and the package and consequently assumes the fonctionnality of the chip. It must bear several loadings during its life time: First of all, it must resist to compressive stress and ultrasonic vibrations during the wire bonding, and afterwards to tensile and shear stresses during the qualification procedure [3]. The reliability of the bond pads has become a major concern with the introduction of new dielectrics and with the continuous downscaling of the pad size. Indeed, the mechanical properties of low-k dielectrics are usually deteriorated as the k value is reduced, due to the introduction of more and more pores into the material [1, 2]. On the other hand, pad size reduction usually leads to loads increase. Experimental results [5] highlight that failure can occur by peeling of the interconnection levels, by cratering into the silicon, or by non-sticking between the top metal layer and the wire (fig. 40). There are several ways to improve pad resistance: To begin with, it is known that material properties play a major role [6, 7]. The wire bond equipment process parameters such as bonding force, ultrasonic power or temperature can also be optimized [8]. However, for a given Front End process flow and a given wire bonding process, pad designing is a key factor, which must be taken into account from the start of an IC design [4, 9]. To get information on fracture modes and crack initiation, a fundamental understanding of these phenomena is required.

Regarding these issues, mechanical modeling is a major tool for the early stages in the development of new wire bond pads. Indeed, simulation enables some low cost design of experiments, and provides insights for technology developments. However, to achieve such targets, an efficient modeling of the bond pad architecture and the whole loads seen by the die is mandatory.

The bond pad architecture is a very complex structure [5]. Moreover, in order to forecast pad failures, the simulated domain must take into account macroscopic loads on the bond pad and then estimate with accuracy the local stress and strain fields in very thin layers. This very detrimental aspect ratio leads to a large amount of elements with a classical FE approach. To overcome this difficulty, it is possible to use the so-called macro-micro technique [6]. This technique has been improved with a first step based on a homogenization technique. The purpose of this particular step is to save CPU time without a loss of accuracy by replacing the meshing of the geometrical details with a suitable modification of the material properties.

The methodology and results aiming at understanding and predicting the bond pad failures are detailed. The problematic and the objectives are briefly presented. Then, the homogenization technique used at the global level is explained and the whole methodology is applied to compare three different bond pad layouts. In conclusion, this paper proposes an efficient modeling methodology to evaluate any bond pad layout.

5.3.1.3 Homogenization technique

Modeling assumptions

During the whole process flow, the bond pad undergoes a wide range of mechanical and thermal solicitations: At the front-end steps, layers are deposited at high temperatures and intrinsic stresses in thin films can induce pre-stressed structures. Nevertheless its impact is assumed to be neglectible as

demonstrated by Mercado and all [6]. The wire bonding process itself consists in the following steps: - First of all a heating of the substrate. - Then a melted gold ball is impacted on the die and an ultrasonic vibration is transmitted through the wire. Inter metallic links between the top layer of the die and the gold wire are thus created [8, 12, 7]. - Finally, to check the integrity of the bond, ball shear and wire pull tests are performed [8, 11].

Thus, both force and thermal loadings are applied to the die, and force solicitation is both quasi static and dynamic. However, since this study focuses on the effect of the layout and comparative results are provides, a linear assumption is used. In particular yielding of the ductile materials, transient phenomena and cumulative effects are not addressed here.

More precisely, 3 independent loads are simulated here: An uniaxial traction or a shear loading on the gold wire, and a uniform thermal variation with an amplitude of 400° on the bonded system, which corresponds to the cooling after the last metal layer deposit.

Figure 1 Example of 3 typical failure modes.

5.3.1.4 Modeling challenge

Typical dimensions of the domain of interest have a very wide range: During the wire bonding process, macroscopic loads are involved by the wire, with dimensions about 50μm corresponding to the wire diameter. On the other hand, the interconnect levels, where the location of the failures investigated here are located, are composed by very thin layers such the hard masks with a typical thickness of 30nm. Moreover, the choice of a three dimensional analysis is prefered to a commonly used plane strain assumption. Indeed, in order to compare with accuracy the bond pad layouts, it is mandatory to be able to make the difference between a via and a metal line, which is not possible in a two dimensional simulation. Thus, to consider this very detrimental aspect ratio would lead to a huge amount of elements with simple FE approach and multi-level modeling need to be performed.

Principle of the multi level modeling

The main steps of multi level modeling are the following:

- Compute a first simulation at global level to get displacements field.
- Locate the maximum strained area, i.e the future location of the micro model.
- Apply the displacement field calculated at the macro level as boundary conditions of the micro model in order to reach the local stress field.

The key point here is to be able to describe the materials and the layout witch compose the macro model with a sufficient amount of details in order to calculate properly the displacement field. At this stage, an homogenization procedure needs to be applied. This enables to take into account the geometrical details by modifying the mechanical properties without meshing all the bond pad layers. However, there are several ways of doing the homogenization step: The most simple one consists in a volumic law of mixture. Although this technique is very easy to use it seems to be insufficient. Indeed, by considering an isotropical description of the multi materials, the eventual orientation of the patterns cannot be taken into account with a mixture law and anisotropic equivalent mechanical parameters need to be considered. Since most of the bond pad structure is periodical, a representative unit cell (RUC) must be chosen. The next paragraph explicits the methodology to apply some periodical boundary conditions as a first part, then the 7 loading cases needed to extract the 9 equivalent mechanical parameters of the RUC as a second part.

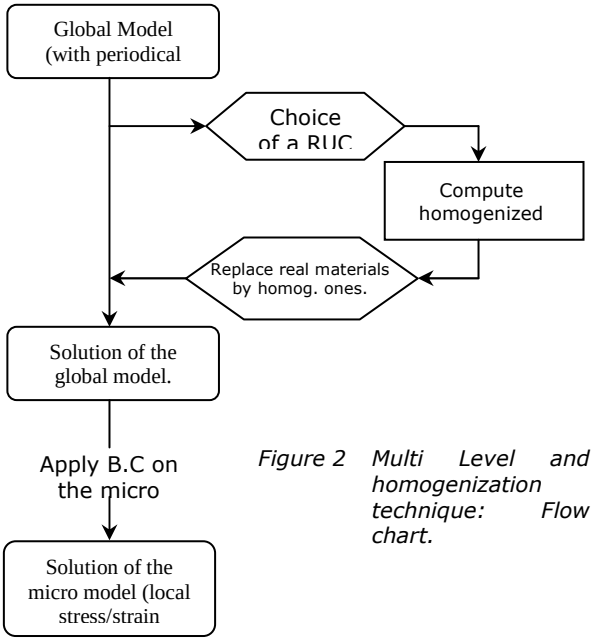

Figure 2 Multi Level and homogenization technique: Flow chart.

Definition of the Representative Unit Cell

The unit cell is described by a parallelepipedic shape with the following dimensions in the *x* x *y* x *z* axes: *(x_max-x_min)*x*(y_max-y_min)*x*(z_max-z_min).* To describe the behavior of the RUC, Hooke's law for orthotropic material in linear thermo-elasticity is written [10]:

$$\varepsilon_x = \alpha_x.\Delta T + \frac{\sigma_x}{E_x} - \frac{\nu_{xy}.\sigma_y}{E_x} - \frac{\nu_{xz}.\sigma_z}{E_x} \quad (1)$$

$$\varepsilon_y = \alpha_y.\Delta T - \frac{\nu_{xy}.\sigma_x}{E_x} + \frac{\sigma_y}{E_y} - \frac{\nu_{yz}.\sigma_z}{E_y} \quad (2)$$

$$\varepsilon_z = \alpha_z.\Delta T - \frac{\nu_{xz}.\sigma_x}{E_x} - \frac{\nu_{yz}.\sigma_y}{E_y} + \frac{\sigma_z}{E_z} \quad (3)$$

$$\varepsilon_{xy} = \frac{\sigma_{xy}}{G_{xy}} \quad (4)$$

$$\varepsilon_{yz} = \frac{\sigma_{yz}}{G_{yz}} \quad (5)$$

$$\varepsilon_{xz} = \frac{\sigma_{xz}}{G_{xz}} \quad (6)$$

with ε_{ij} ($i \neq j$) the engineer shear strain, i.e. the total shear strain : $\varepsilon_{ij} = \frac{\partial u_i}{\partial x_j} + \frac{\partial u_j}{\partial x_i}$.

Displacements of the RUC have to be input on the master nodes and each node of the exterior surface is coupled with the corresponding node of the opposite face and to the master node of the considered face. To prevent rigid body motion, point O is locked in the three directions whatever the loading case.

Considering:

- a node *P* located on one of the 3 exterior surfaces of the model: $P=\{x_{max},y,z\}$ or $P=\{x,y_{max},z\}$ or $P=\{x,y,z_{max}\}$.
- *Master_P* is the master node of the face where the P node is.
- *P'* is the node at the opposite of the node P.

- The vector $U=\{u,v,w\}$ describes the displacements of any node P (i.e. DOF solutions).

Each node of the exterior surface is coupled with the opposite one and the master node with:

$$\boxed{U_P = U_{P'} + U_{Mst\_P}} \qquad (7)$$

Hence, resulting deformed shape is consistent with periodical boundary conditions.

Homogenized properties computation

To extract the equivalent orthotropical properties, some particular loading cases leading to a simple stress and strain state are applied, i.e:

- 3 tensile loads give Young's moduli and Poisson's ratio: E_X, E_Y, E_Z, ν_{XY}, ν_{XZ}, ν_{YZ}.
- 3 shear loads give shear moduli: G_{XY}, G_{XZ}, G_{YZ}.
- 1 thermal load provides coefficients of thermal expansion: α_X, α_Y, α_Z.

In addition to the couplings described in *2.4*, the following boundary conditions are applied on the master nodes (noted *'Mst'*):

Loading case #1: X-wise traction

$$U_{Mst\_x}=\begin{Bmatrix} u\neq 0 \\ 0 \\ 0 \end{Bmatrix} \quad U_{Mst\_y}=\begin{Bmatrix} 0 \\ free \\ 0 \end{Bmatrix} \quad U_{Mst\_z}=\begin{Bmatrix} 0 \\ 0 \\ free \end{Bmatrix}.$$

From (1) and (2), it comes:

$$\varepsilon_x = \underbrace{\alpha_x.\Delta T}_{=0} + \frac{\sigma_x}{E_x} - \underbrace{\frac{\nu_{xy}.\sigma_y}{E_y}}_{=0} - \underbrace{\frac{\nu_{xz}.\sigma_z}{E_z}}_{=0} \Rightarrow \boxed{E_x = \frac{\sigma_x}{\varepsilon_x}}$$

$$\varepsilon_y = \underbrace{\alpha_y.\Delta T}_{=0} - \frac{\nu_{xy}.\sigma_x}{E_x} + \underbrace{\frac{\sigma_y}{E_y}}_{=0} - \underbrace{\frac{\nu_{yz}.\sigma_z}{E_z}}_{=0} \Rightarrow \boxed{\nu_{xy} = -\frac{\varepsilon_y.E_x}{\sigma_x}}$$

Loading case #2: Y-wise traction

$$U_{Mst\_x}=\begin{Bmatrix} free \\ 0 \\ 0 \end{Bmatrix} \quad U_{Mst\_y}=\begin{Bmatrix} 0 \\ v\neq 0 \\ 0 \end{Bmatrix} \quad U_{Mst\_z}=\begin{Bmatrix} 0 \\ 0 \\ free \end{Bmatrix}$$

From (2), it comes:

$$\boxed{E_y = \frac{\sigma_y}{\varepsilon_y}}$$

Loading case #3: Z-wise traction

$$U_{Mst\_x}=\begin{Bmatrix} free \\ 0 \\ 0 \end{Bmatrix} \quad U_{Mst\_y}=\begin{Bmatrix} 0 \\ free \\ 0 \end{Bmatrix} \quad U_{Mst\_z}=\begin{Bmatrix} 0 \\ 0 \\ w \end{Bmatrix}$$

From (3) and (2), it comes:

$$\boxed{E_z = \frac{\sigma_z}{\varepsilon_z}}$$

$$\boxed{\nu_{yz} = -\frac{\varepsilon_y.E_y}{\sigma_z}}$$

$$\boxed{\nu_{xz} = -\frac{\varepsilon_x.E_x}{\sigma_z}}$$

Loading case #4: XY shear

$$U_{Master\_x} = \begin{cases} free \\ v \neq 0 \\ 0 \end{cases} \qquad U_{Master\_y} = \begin{cases} 0 \\ free \\ 0 \end{cases}$$

From (4), it comes:

$$\boxed{G_{xy} = \frac{\sigma_{xy}}{\varepsilon_{xy}}}$$

Loading case #5: XZ shear

$$U_{Master\_x} = \begin{cases} free \\ 0 \\ w \neq 0 \end{cases} \qquad U_{Master\_z} = \begin{cases} 0 \\ 0 \\ free \end{cases}$$

From (5), it comes:

$$\boxed{G_{xz} = \frac{\sigma_{xz}}{\varepsilon_{xz}}}$$

Loading case #6: YZ shear

$$U_{Master\_y} = \begin{cases} 0 \\ free \\ w \neq 0 \end{cases} \qquad U_{Master\_z} = \begin{cases} 0 \\ 0 \\ free \end{cases}$$

From (6), it comes:

$$\boxed{G_{yz} = \frac{\sigma_{yz}}{\varepsilon_{yz}}}$$

Loading case #7: Thermal loading

$$U_{Mst\_x} = \begin{cases} free \\ 0 \\ 0 \end{cases} \quad U_{Mst\_y} = \begin{cases} 0 \\ free \\ 0 \end{cases} \quad U_{Mst\_z} = \begin{cases} 0 \\ 0 \\ free \end{cases} \text{ and } \Delta T \neq 0$$

From *(1)*, (2) and (3), it comes:

$$\boxed{\alpha_i = \frac{\varepsilon_i}{\Delta T}} \text{ with } i = x, y, z.$$

In this section, 7 loading cases have been defined and deformed shape, stress and strain fields are now known and enable to extract to 9 equivalent mechanical properties of the unit cell.

Note 1: There are two ways to evaluate the global value of stress and strain, both lead to the same result: Either the element values of $\varepsilon_i, \sigma_i, \varepsilon_{ij}, \sigma_{ij}$ are averaged on the whole model, taking into account element volume weighting, or the reaction forces are extracted from the master nodes, where displacements are imposed.

Note 2: It should be kept in mind that restrictions are assumed on the description of the simulated structure behavior: In deed, the unit cell is not considered as fully anisotropic but only 9 coefficients of the stiffness matrix are computed. For example, no coupling between traction and torsion is performed.

5.3.1.5 Impact of the homogenization step: Effect of the unit cell

Description of the 3 approaches

This section concerns the modeling at the macro scale. This demonstrates that the unit cell must be properly chosen to ensure that accurate results are provided in terms of displacements at the macro scale. More precisely, the aim is to find the most appropriate technique to evaluate the displacements in the macro model regarding:

- the accuracy of DOF calculation.
- the accuracy of stress/strain field induced in the micro model.
- the CPU time and complexity to build the model.

The bond pad is compound by a stacked structure of via layers and metal layers. Via layers are mainly made with dielectrics, whereas metal ones are mainly compound by copper. By consequence, some soft and hard layers alternate and mechanical properties are quite different from one layer to the closest one. According to 2 different kinds of loads (force and uniform thermal variation), 3 approaches are compared:

- The reference approach consists in a coarse meshing of all the geometrical details. The memory usage of such a FE model is very large and very complex layouts can not be modeled with such an approach.
- The next approach named "Homog. I" uses the homogenization methodology previously explained and considers as the unit cell the full stack of interconnect layers at once. This approach is very attractive because neither the geometrical details nor the thin film thicknesses need to be meshed.
- The last approach is an intermediate case: Indeed the homogenization procedure is only applied for the in-plane description, and the out of plane discretization remains. Thus, there are as many unit cells as metal and via levels. This "Homog. II" named model is also very attractive in term of computer resource.

Modeling of the inner pad	Geometrical details	Material properties	CPU usage
Reference	Yes	• Isotropic • 1 per material	
Homog. I	No	• Orthotropic • 1 for all layers	 
Homog. II	Partial	• Orthotropic • 1 per layer	

Table 1 Comparative table of the 3 homogenization approaches.

Description of the tested structure

The tested bond pad structure chosen to evaluate the calculated displacement in the global model regarding the 3 different approaches is made of 6 metal layers. More precisely, the metal layers are full plates with small holes in them, and there is no via in the inter metallic layers.

The loads simulated here are either a combination of pull and shear loading or an uniform thermal variation.

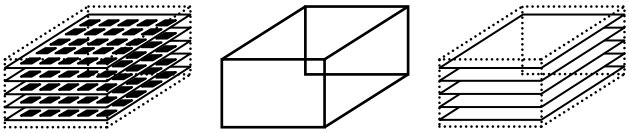

Figure 3 Schematic view of the 3 macro models (left: Reference case with a full details discretisation; center: Homog. I with 1 orthotropic material for all the layers; right: Homog. II with 1 orthotropic material per layer).

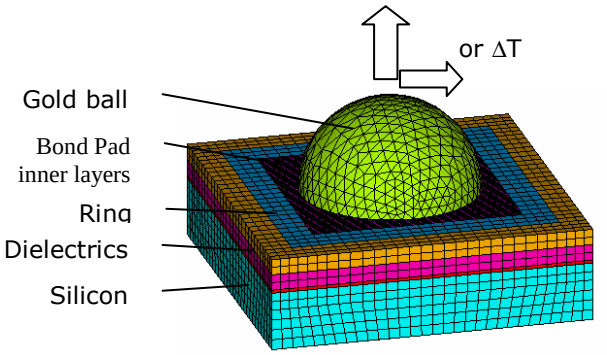

Figure 4 Global model overview.

Results

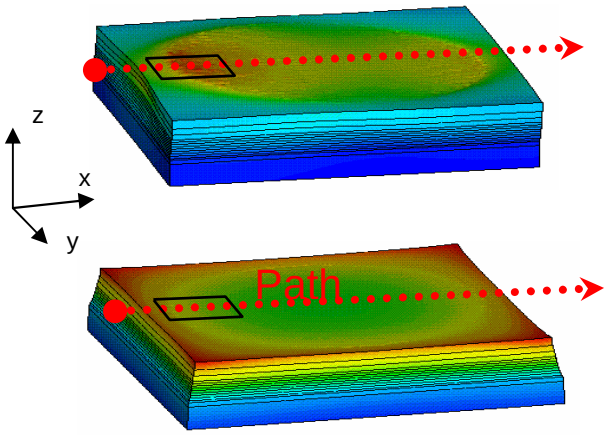

Figure 5 Example of a calculated displacements field (sum of all DOF) of the bond pad layers. Pull and shear loadings combined (top), Thermal loading (bottom). Red arrows show a path at the interface ball/top of the pad. Black squares locate the position of the micro model.

Figure 6 shows that the 3 approaches provide very different results. Indeed, 2 components of the displacement (those in the loading directions) are plotted and results highlight that the case "Homog.II" gives a quite similar solution as the reference case whereas the results from "Homog.I" are far from the real solution. I.e the homogenization layer by layer gives a better accordance than the homogenization of the full thickness.

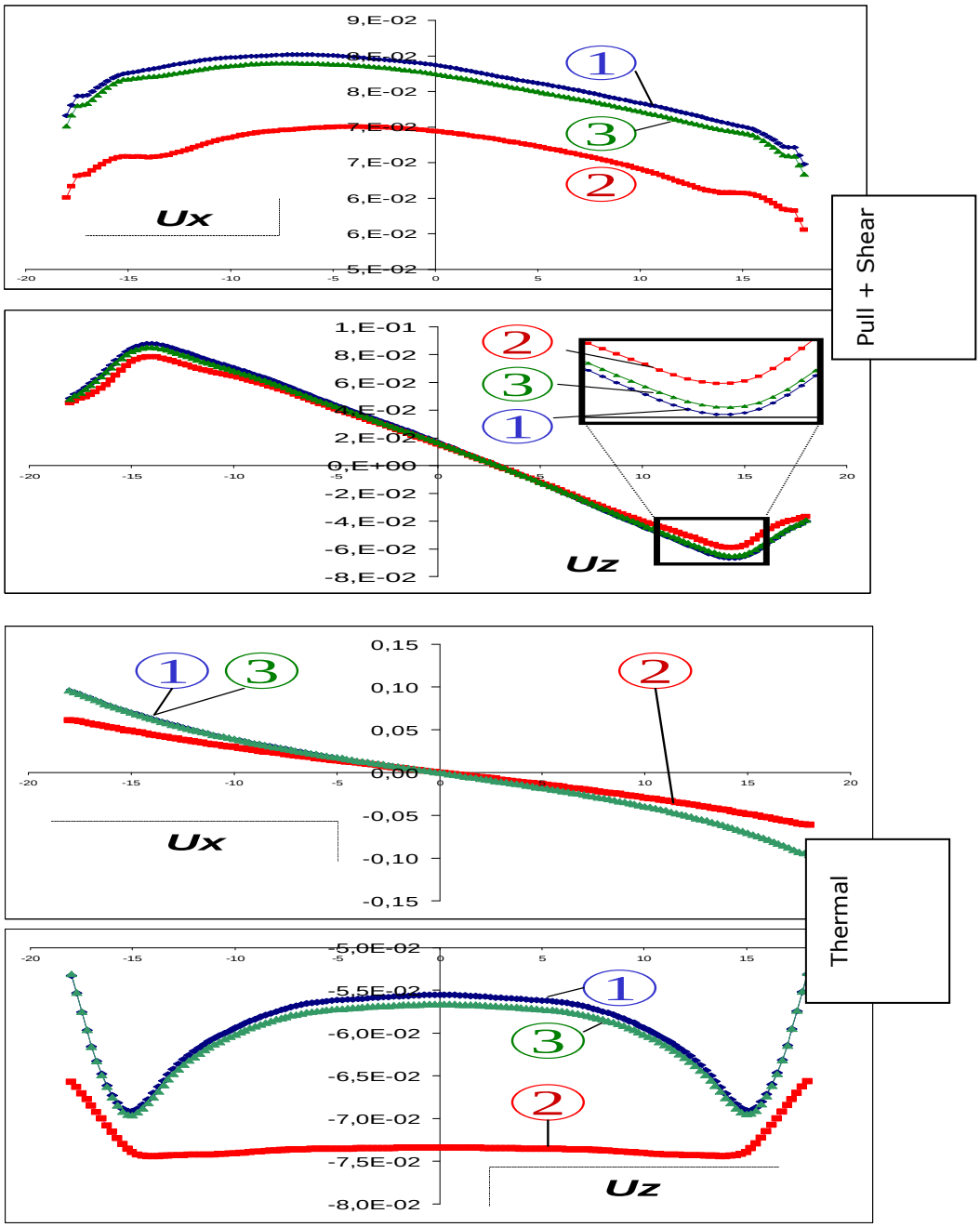

Figure 6 Tangential (Ux) and normal (Uz) displacements for the 3 approaches (1: reference, 2: Homog.I, 3: Homog.II) and for pull+shear loading (top) and thermal loading (bottom)

Since in a multi level modeling the final aim is to reach the local stress/strain field, the key point is to evaluate if the resulted local fields calculated in the micro model differ according to the approach chosen to discretize the macro model. Figure 7 shows the equivalent Von Mises stress field calculated for a micro model composed by a single material. Such a micro model is chosen for viewing and testing purposes only, as it enables to illustrate in 3 dimensions the derivative of the displacement field. The location of the micro model is drawn on fig. 4 and corresponds to the location of the maximum strain in the macro model.

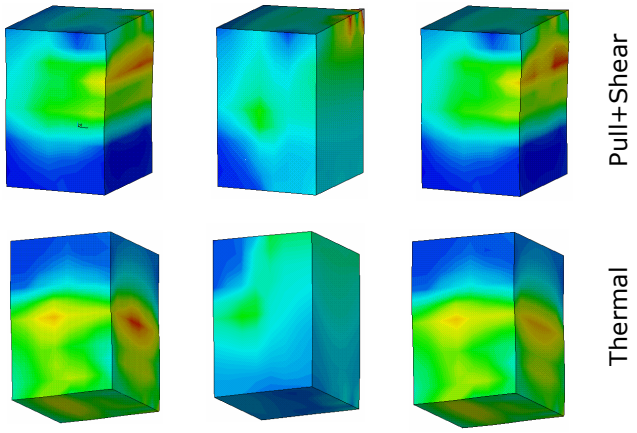

Figure 7 *Von Mises equivalent stress field calculated from the 3 approaches at the local scale (left: from reference case, center: from Homog.I, right: from Homog.II) and 2 loadings (top: Pull+Shear, bottom thermal).*

Fig. 7 confirms that the 3 approaches lead to very different results. Indeed, the homogenization layer by layer (Homog.II) results are very close to the reference case. Moreover, it is obvious that by homogenizing all the pad layers at once (Homog.I), local strain concentrations are not captured.

Finally, like in a whole multi scale approach, the displacement field is applied as boundary conditions of a micro model where the geometrical details are described. Then, the average stress is computed in the low-k material and compared to the one calculated from the reference approach for the two loading cases. Results in table 2 show that the layer by layer homogenization provides accurate results, whereas errors resulting from the orthotropic mixture law (Homog.I) are quite large.

	Pull+Shear		Thermal	
Ref. vs.	Homog.I	Homog.II	Homog.I	Homog.II
σ_1	18%	3%	29%	2%
σ_{VM}	19%	3%	14%	4%

Table 2 Comparison of the average stresses (σ_1:1st principal, σ_{VM}: equivalent stress) calculated in the dielectric material.

Hence, the both loading cases give the same conclusion: The homogenization technique allows to save CPU time and makes easier the model building and meshing. However, the unit cell must be chosen carefully and results highlight that: - To consider only 1 RUC in the thickness direction leads to an inaccurate estimation of the displacement. By consequence, stress/strain local fields in a macro/micro analysis will be wrong. - By choosing 1 RUC for each layer, results are very similar compared to the real solution given by the meshing of all the geometric details.

In the next chapter, the exposed homogenization method added with a multi-scale FEM will be used aiming at comparing several pad architectures regarding their resistance to the wire bonding process.

5.3.1.6 Application: Comparison of wire bond pads

Wire bond pads description

In this section, the previously exposed methodology is applied in order to numerically compare 3 different layouts regarding their resistance to wire bonding. The 3 bond pads can be described as:

- Pad #1: Slotted short metal lines and vias at interconnect levels.
- Pad #2: Long lines, oriented in a single direction per metal level and rotated from a layer to the upper one. Vias are also drawn in this bond pad.
- Pad #3: Metal plates with small holes (similar to the tested structure in the previous paragraph) and no via.

Experimentally it is found that structure #1 presents a high percentage of peeling failures during the wire pull test, whereas the 2 others reach the specifications of wire pull and ball shear tests.

3 loading cases are independently applied on these models. Hence, the contributions of the wire pull test, the ball shear test and an uniform thermal variation are split.

Macro scale results: Location of the most strained area according to the loading cases

The results at the macro scale does not show large differences between the compared architectures. However, it can be noticed that the most strained area at the macro scale is very dependent of the loading case. More precisely, the likely locations of failures are located at the edges of the pad layers for the thermal loading, at the center of the bond pad for the pull test, and at the edge of the foot print of the gold wire for the shear test (fig. 8).

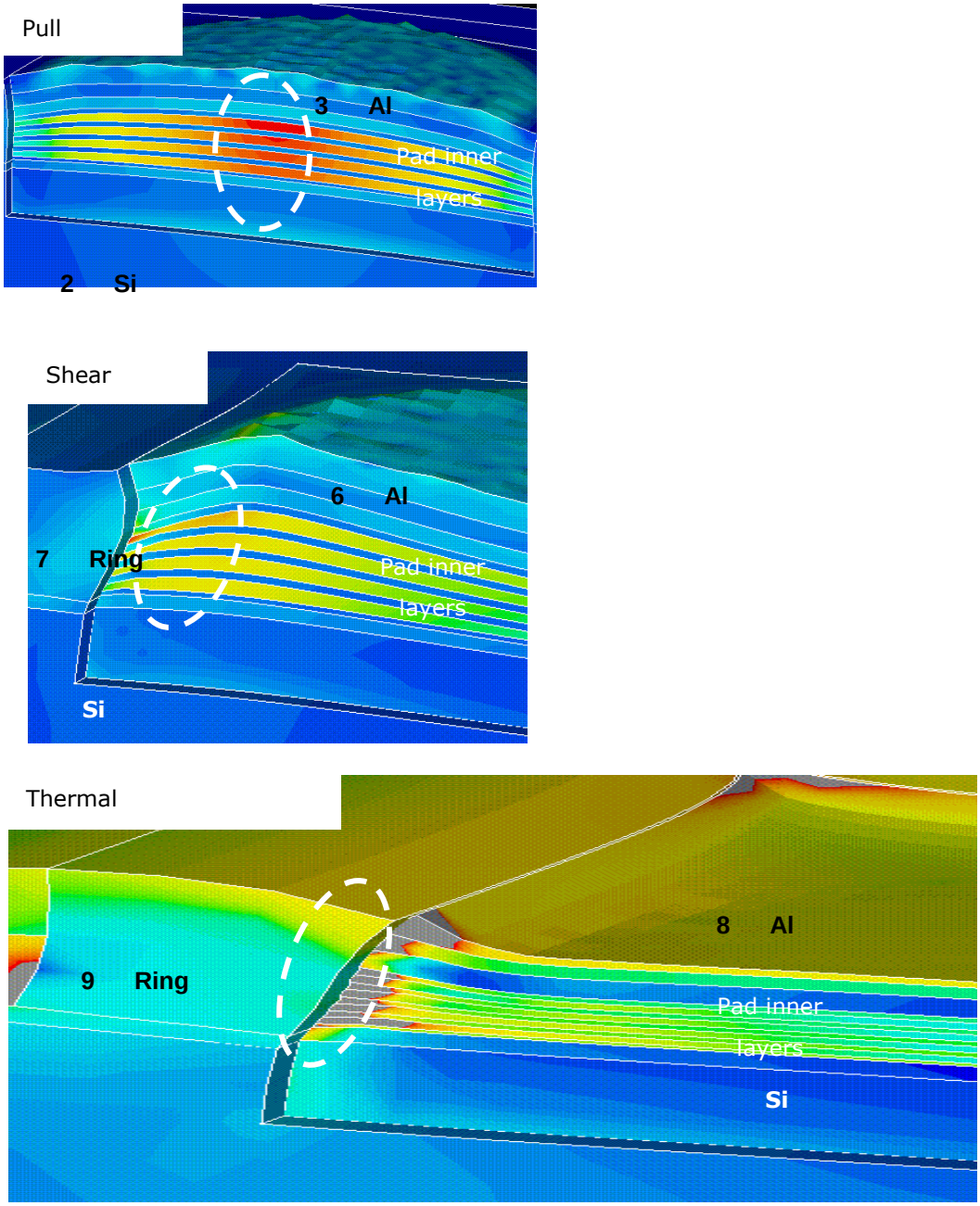

Figure 8 *First principal strain component figure in a cross section of the half pad. For viewing purpose gold wire has been removed and deformed shape is scaled.*

Local scale results: About failure criteria and architectures comparison

One of the main issues in mechanical modeling is to find the suitable criterion that corresponds with the observed failures. Thus, there are several ways to post-process given calculated stress and strain field and, in our case, the evaluation of the different bond pads could be affected by the choice of the failure criteria. Experimental observations show that crack nucleation occurs in the dielectric layers, hence our attention is focused on the low-k material. The first principal stress component is closely analyzed. Indeed, fig. 9 represents the volumic stress distribution of the first principal stress component according to the loading case and the 3 compared structures. Some information can be

extracted from this plot: The extrema values, that give some input concerning crack nucleation, as well as the curve shape representing the volumic proportion of low-k material that undergoes a certain amount of stress, which is related to the risk of crack propagation. Hence, the more the plot is on the left side, the more the structure would resist to the considered loading.

As shown in fig. 9, one of the architectures gives much better results than the two others. Indeed, architecture #2 has both extrema and averaged stress values lower than #1 and #3. On the other hand, #1 has the highest maximum stress values but the plots are generally on the left side of #3 (i.e a higher level of stress). Hence, for these two architectures the classification is more subject to discussion but since the maximum values are much higher in #1 than in #3, the architecture #1 should be the worst one regarding the resistance to wire bonding.

Concerning the contribution of each loading case in a wire bonding failure, this work shows that the highest stress levels are induced by the thermal loading. Hence, it is likely that the peeling or cratering cracks experimentally observed are in fact initiated at certain steps preceeding the wire pull test. Among presently tested loads, the most damaging one is the thermal variation involved during the building of the bond pad.

5.3.1.7 Conclusions

This work proposes and details an efficient methodology to numerically evaluate wire bond pad architectures.

The use of a multi level modeling enables to simulate the loadings that are applied at the global scale and also to capture the local stress field in some three dimensional patterns. However, the importance of the unit cell used in this step is highlighted. Indeed, one shows that a simple mixture law is not sufficient to accurately evaluate the displacements in the macro model and, by consequence, to calculate the stress field in the local model. Thus, by taking precautions, the application of the method to a wide range of architectures is allowed.

The different kinds of loads seen by the bond pad (thermal variation and force loading) are modeled in a linear three dimensional analysis and the contribution of these loadings is discussed. The location and the value of the maximum stress are found to be dependent of the loading case. Furthermore, results highlight that by modifying the bond pad layout, stress level and by consequence risk of failure can be reduced. Thus, three different pad architectures are numerically evaluated and ranked. On the other hand, it is found that whatever the bond pad layout, the thermal loading appears to be the major stress contributor compared to the wire pull and ball shear tests. Indeed, the stress induced by the process steps seems to be one of the root causes of crack nucleation. Hence, concerning the experimentally observed bond pad failures, wire pull and shear tests act on the propagation of previously created damages.

Acknowledgments

Thanks are due to Philips CFT people in particular Ruud Voncken; Cindy Goldberg from the Alliance Pad Module team and F.Quercia team from ST Packaging Grenoble.

5.3.1.8 References

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5.3.2 Chip-Package Interactions: Some combined package effects on Copper/Low-k Interconnect Delaminations

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5.3.2.1 Abstract

The introduction of brittle dielectric materials, and the feature size decrease of IC chips to follow Moore's law, are well known to pose great integration challenges. In this paper, a 3D fully parameterized Finite Elements of a Ball Grid Array package model is built and thermo-mechanical stress produced during package operations is evaluated. That aims to address FE-BE compatibility concerns. Thanks to multi level and energy based post processing methods, both analysis at the package and interconnect levels are carried out. The preliminary analysis at the package displacements and comparison with measurement maps allow to validade the package model. Localized evaluation of the crack propagation likelihood into the low-k stack underlines the particular effects of the glue fillet geometry and die attach thickness. On the other hand a drastic rise of the fracture risk is suspected with highest values of the glue fillet, and for the considered configurations, with thinest die attach. The sensitivity to shear modes, contrary to compressive one is highlighted, and released energy plots indicate an higher delamination hazard in the bottommost IMD layers. Possible extended applications of this work are the early phases of technology developments and product crisis solving.

5.3.2.2 Introduction

Aiming to improve product performances and size reductions, die interconnect features are commonly driven by electrical specifications. Among others, that leads to critical dimension decreases and new material integrations [1]. Hence, the so called Cu/Low-k couple in interconnects is nowarday widely used to reach RC specifications. However, to lower the k value the introduction of nanometric pores in dielectric materials causes weaker mechanical strenght of the die stack [2]. Hence, beyond the FEoL integration issues of low-k and ultra low-k insulators, die interconnect failures are now commonly observed during packaging tests and qualifications [3, 4]. More precisely, interfacial delamination and cracking in BEoL during packaging occur. By consequence, front and back end processes can not be separated anymore and close interactions of die and package features must be accounted as a great integration challenge [5].

Modeling is one of the major tools to understand and reduce mechanical related defects, to save trials on actual silicon, and to allow early stage development and crisis solving. However, such simulation remains a challenge and both the geometrical and failure caracteristics involved require specific methodologies [6, 7].

In this paper, starting from observations on product, simulation works are carried out to understand failure mechanisms. First of all, package warpage measurements at distinct temperatures are faced to numerical results in order to validate the displacement states. Then, the analysis is focused at the fine scale of the low-k interconnects. More precisely, the specific effects of the die attach features on chip-package interactions are investigated. Starting from experimental insights, modeling results on low-k delaminations are hence discussed. Failure hazard, location within the stack, and risk mitigations with respect to some of the package parameters are particularly studied.

5.3.2.3 Typical observed failures

As introduced, packaged products have been submitted to thermo cycles in order to achieve a complete process qualification. These reliability tests performed during the early qualification stages with unoptimized package parameters revealed abnormally high failure rates. Analysis of the accoustic and electrical responses on failed parts determined that the location of the delamination is situated at the die corner. Then, FIB cross sections have been carried out on the die to locate more precisely the involved interface. In most of the cases, the lower part of the Inter Metallic Layers was the location of

the main path for crack propagation. Figure 41 depicts a typical delamination occurrence, showing obviously the fracture propagating trought first metal and dielectric layers.

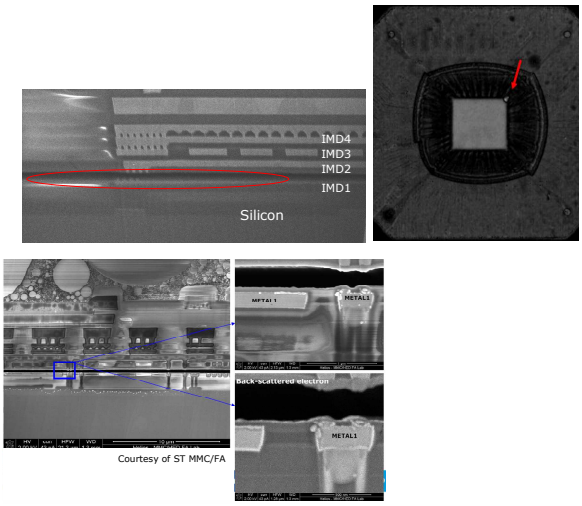

Figure 41: Cross section view of typical delamination observed in interconnects after packaged thermo-cycle tests.

In a second phase, process and parameters optimization enabled to fit with reliability spectifications; and; among others, yield values were significantly increased by a better management of the die attach features.

In the next sections, modeling strategy will be depicted, and results faced to both the warpage measurements and the below mentionned experimental failure analysis.

5.3.2.4 Modeling methodology

Multi scale modeling

As previously introduced, the dimension ratio from package to interconnects is about 1/500,000. It is impossible to use a single finite element model to simulate the detail of the interconnection features without a super-computer. Fortunately, sub-modeling techniques can be used to deal with this kind of problem with less computation effort.

The concept of sub-modeling is to build several models. The first one is a global model with relatively coarse mesh pertaining to the global boundary conditions (BC). The second one is called a sub-model, containing a detailed mesh for the specific area of interest. The sub-model's BC is inherited from the global model by interpolating the nodal displacements and body forces from the global model. The accuracy of the sub-model is dependent on the coarseness of the global model and the details of the sub-model. For the current problem, despite an high amount of finite elements, reliable accuracy has been obtained by the use of only two fine meshed models: A package and interconnect ones. The package model is used to assess to stress applied to the die part, and the last sub-models relates to silicon features, describing copper/low-k layout. In the first model, reliable description of the true behaviour of the die is achievied thanks to homogenisation technique, allowing to consider local design. Figure 42 shows the multi level methodolgy and homogenization flow chart.

This later thing is one of the key points of the multi-level modeling technique, i.e. the evaluation of the equivalent properties of the materials. Among the required steps, the choice of the representative unit cell (RUC) used for the homogenization is of the utmost importance. Indeed, depending on the RUC, an inaccurate evaluation of global level displacements may occur, leading to errors in the local level calculated stress and strain fields. The complete homogenization procedure used for the interconnect layers was previously studied and reported [8]. More precisely, it was shown that a simple volume averaging is unable to render the anisotropic behavior of the interconnects and that a independent discretization of the Inter Metal Dielectric (IMD) layers is mandatory.

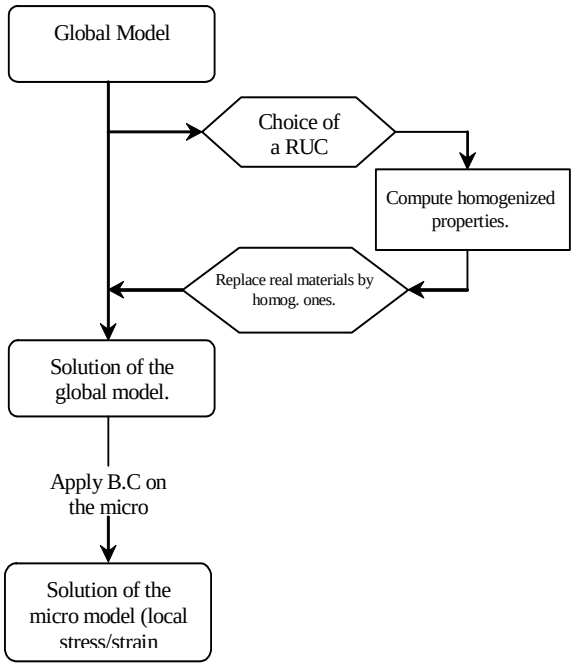

Figure 42: Multi Level and homogenization technique: Flow chart.

5.3.2.4.1 Fracture Mechanics

Once the strategy for the finite element models has been defined, suitable criteria must be chosen according to the observed failure modes and by taking into consideration the behavior of the material set used. Despite the fact that in-situ observations of the failure modes are tricky, the most likely scenario in our case is brittle fractures. Furthermore, micro-cracks are highly suspected to nucleate at the early stage of packaging steps such as sawing processes, which initiates local defects at the many interfaces of metal layer and low-k dielectric. Hence, the targeted failure mode, which is brittle delamination, is related to fracture mechanics and specific energy based numeric tools are developed [9, 10]. The so-called Nodal Released Energy (NRE) post processing procedure is based on the computation of energetic quantity from the nodal solution. To evaluate the NRE value, two simulations are required: One with an undamaged model, the other with the damaged one where a virtual crack has been inserted.

At this step the crack features need to be defined, particularly in terms of size and shape.

This method, easily implementable in commercial Finite Element software, enables to provides energy based quantities of the distinct opening crack modes even in complexe 3D models. Figure 43 shows the post processing flow chart and formula.

Note that the numerical parameters to be used, the sensitivity and the ability to link this value with the energy release rate has been previously validated; and additional insights compared to a standard stress based analysis have been previously demonstrated [8].

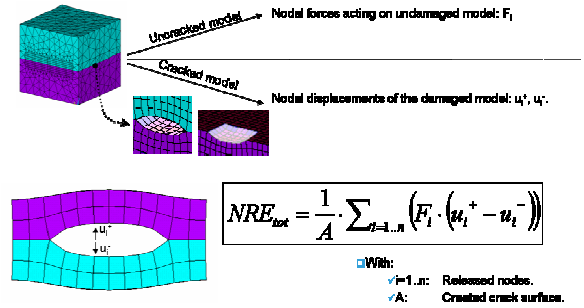

Figure 43: Nodal Release Energy (NRE) flow chart and formulae.

5.3.2.4.2 Models

Finite elements models

Global and local finite elements models are now built. Note that, to allow further industrial design optimizations, models are parametrized and three dimensional.

The main features of the models are as follows: For the global one, package type is BGA, using parts described in Table 3. The local interconnect model depicts the typical stack of an advanced CMOS90 product. The simulated die stack is seven copper metal levels (7ML) including five low-k

Table 3: Main reference model features.

		Dimension Package [mm] Interconnects [µm]	Young's modulus @[°]:[GPa]	Poisson's ratio	Coefficient of Thermal Expansion @[°]:[ppm/°]
Package	Core	13 x 13 x 0.22	19	0.3	In plane: 16.9 Out of plane: 30
	Die	6.5 x 6.5 x 0.17	130	0.28	3
	Die attach	0.02	100	0.3	0.13
	Molding compound	0.67	24	0.4	8
Interconnect	SiO2	2 thick levels + PMD	48	0.3	2.67
	Low-k	5 thin levels	8	0.15	15
	Copper		128	0.33	16.6
	Nitride		164	0.24	2.67

levels and the two others containing classical silicon dioxide as dielectric. Figure 44 depicts the two models used in the multi scale simulation, a meshed interconnect pattern is provided as an example. In addtion, preliminary analysis shown that the starting location of the failure is situated at the die corner, where specific design rules are applied. Hence, models in both modeling levels account for the particular interconnect structure in that region thanks to homogenization technique and detailled meshing.

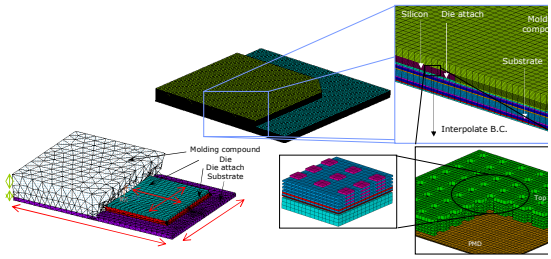

Figure 44: Package and interconnect Finite Element models.

Package warpage figures

In order to enhance confidence in the finite element model of the package, a first step aims to face numerical displacement plots with measurements. Hence, the package warpage is monitored during thermo cycles from high temperatures to ambient. The package warpage values at distinct temperatures are plotted in . These results allow to validate the package simulation, since both values

and curve shape are well reproduced. More precisely a smiling package warpage is found at high temperature, which becomes crying while temperature decreases. In addition, as depicted in Figure 46, it might be guessed from the experimental figures that package shape is double bended. This feature is also confirmed by simulation.

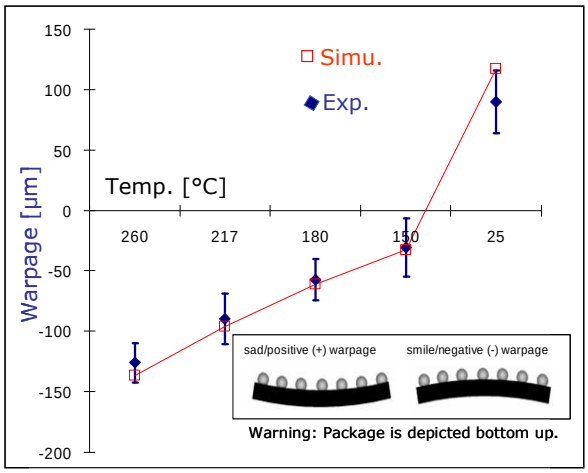

Figure 45: Comparison between experimental and simulated package corner displacements at distinct temperatures.

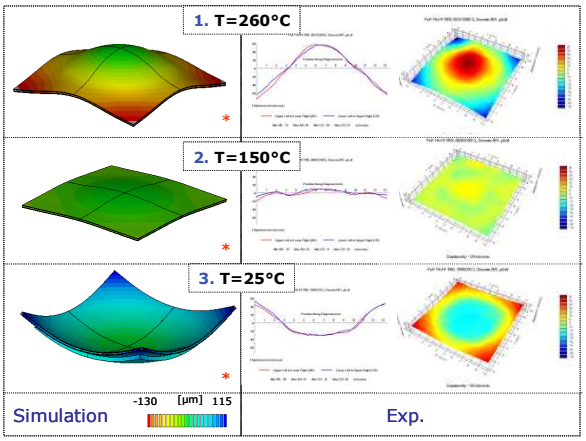

Figure 46: Comparison between measured (right) and simulated (left) package displacements figures at 260°C (top), 150°C (middle) and ambient temperatures (bottom).

Loading conditions

An uniform thermal variation from +150 to -40°C is applied to reproduce the thermo cycling which causes the delaminations. Coeficient of thermal expansion (CTE) mismatch of materials induces device warpage and generates stress into interconnect. Actually, the likely physic governing crack propagation is here fatigue related. However, since modeling strategy is driven by the targeted application, a compromise must be made with industrial requirements. By consequence on this work, which is oriented on process and complexe structure optimization and root cause seeking, a linear fracture mechanics approach is prefered. The main drawback of this approach remains the unability to provide lifetime prediction and quantitative variations of failure rates. Thus, uniform thermal variation corresponding to the cooling amplitude is applied, and materials are considered as stress free at initial temperature.

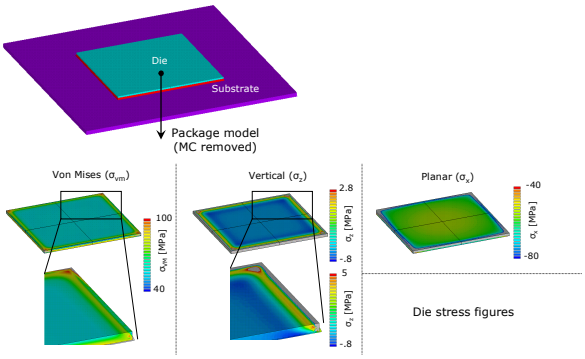

Figure 47: Die stress at global level.

5.3.2.4.3 Simulation results

Package level analysis

At first, package stress and deformation are analyzed at the global level. Note that deformed shape can be differents depending on package parameters ; In our application case, figure is crying with a maximum vertical downward displacement of about 100µm at the device corner.

Throught package deformations, die stress is generated. Figure 47 shows silicon figures and results underline a quite constant compressive deformation field in the main central region of the die. More precisely, a highly planar compressive stress is found, whereas vertical component remains limited. On the other hand, stress gradients are specially observed at the die corner, where Von Mises stress becomes significant, revealing presence of shear stress components.

A deeper analysis highlights that die corner stress features are particularly affected by the die attach geometry. In order to precise these effects, several die attach geometries are simulated and stress plots are depicted in Figure 48. Results confirm that the edge regions of the die are mainly impacted, whereas the central stress field is left quite unchanged. Three die attach configurations are

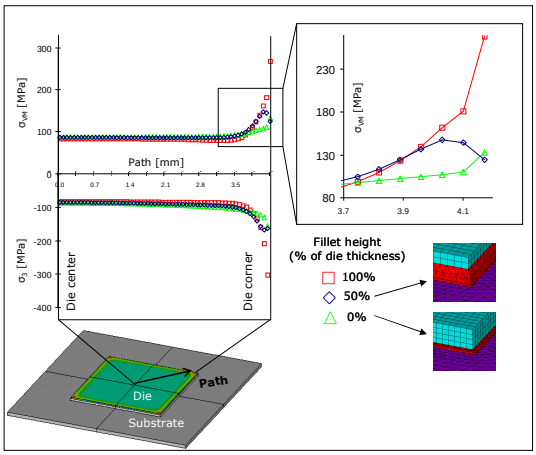

Figure 48: Package level analysis: Von Mises and compressive stress components at top die according to fillet geometry.

compared: The glue fillet height ratio between bottom and top silicon ranges from a null to a full value, and a medium case depicts a glue fillet edge coming up to the half of the silicon. Plots show that, depending on the height, both corner peak stress value and stress distribution at the die edges and corners are strongly modified. In addition, it is particularly interesting to observe that a secondary maximum stress value is located in the inner part of the die, and not only limited to the edge and corner singularities. Note that this feature could have a link with the delamination failures. Indeed, considering that the extreme edge of the silicon is compound by the sawing street, micro cracks confined in that region and at least at the first order, should not affect the reliability. However, stress in the active part of the die could be much more critical for reliability. Thus, by generating an higher

stress at a distance of about 200µm from the corner and hence just into the seal ring structure, the glue fillet geometry is suspected to play an important role in crack propagation during packaging tests.

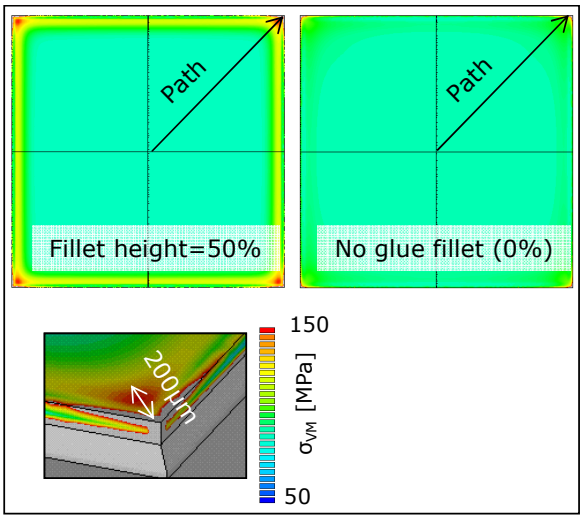

Figure 49: Package level analysis, top view of Von Mises stress at top die for the two extreme configurations of glue height.

Figure 49 compares the plane view of the stress field with the two extrem configurations of the glue fillet, revealing that peak stress is shifted inside the die. In addition, the principal stress vectors generated close to the glue edge are depicted in Figure 50.

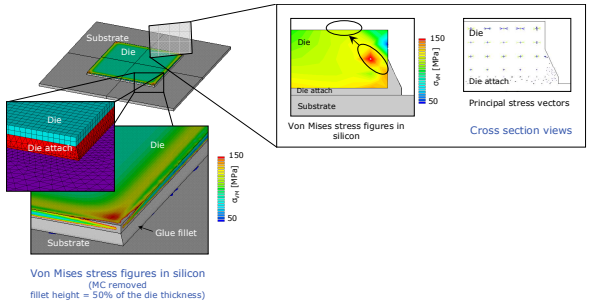

Figure 50: Package level analysis, in plane and cross section view of stress features at die corner.

Energy based analysis at low-k level and discussion

Once package stress and the specific effect of the die attach have been analyzed at the global scale, deeper investigations are then carried out in the interconnect model and using the previously described energy based index. The multi scale parameters are determined thanks to the package analysis. In particular, the location of the local model is put in the seal ring region, in where peak stress and failures are indeed observed.

Values of the nodal release failure index for the interconnect interfaces are plot in Figure 51. Interface numbered 1 corresponds to the bottomest layer (i.e. between the first metal and via level) and the interface numbered 4 represents the top last low-k/copper level). Variations with respect to the glue fillet height, in percentage of the total silicon thickness, and the die attach thickness are respectively depicted throught the planar axes from 10 to 40 µm.

Generally speaking, despite the fact that the main part of the energy values are attributed to the first crack opening mode (i.e. for this loading condition a compressive component), variations are obtained throught the shear components. As a first consequence on the damaging mode of the used low-k material, compressive stress state would not lead to weaken low-k interface. The intrinsic porous feature of the material structure, which could have made it sensitive to crushing phenomena, is obviously questionnable. Hence, fracture occurrence would be here rather related to crack propagation thank to shear opening modes. As a general remark, it must be noticed that in any simulation, notably

because critical adhesion values are strongly dependent on the mode mixity, the most relevant criteria to account remains a key concern for modeling.

More specifically, with our tested cases, the local analysis draws trends and allows several insights:

Firstly, the glue fillet height is confirmed to be a major parameter, since energy values increases drastically while the fillet reachs the top silicon region. However, delamination risk are left quite unchanged if keeping glue fillet at a sufficiently low value, and limited variations are obtained in case of fillet remains in the bottom half of the silicon height.

On the other hand, for a given glue geometry, the effect of the die attach thickness is revealed. Despite the low CTE of the material, it is found that the use of a thicker glue layer leads to lower the risk. It must also be noticed that this insight is really dependant of product features. More precisely, in some other applications using other bill of materials, effects could be reversed, and a dedicated analysis is mandatory.

In addition, the NRE values are mitigated considering the interconnect level. Indeed, contrary to engineering feeling suggestions, the middle region of the low-k stack is in all cases the most suceptible to failure. Indeed, modeling results in the criticalest configuration determine the second interface as the worst one. Note that this specific feature is confirmed by experimental cross sections of failed products, which reveal that the delamination, in the most often cases, propagated in between the first or second inter metal dielectric layer.

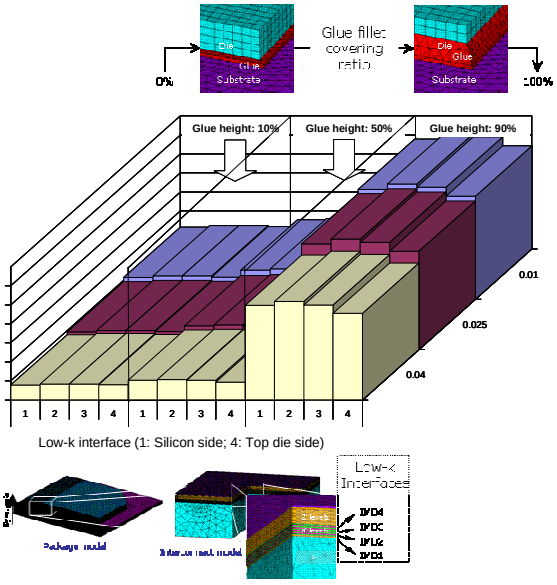

Figure 51: Interconnect local analysis: Nodal Release Energy values in low-k layers, according to glue fillet covering ratio and die attach thickness.

5.3.2.5 Conclusions

Motivated by yield loss during qualification tests and based on experimental investigations, thermo-mechanical simulations have been carried out to address some chip-package interaction concerns. In this paper, the dedicated modeling methodology, including multi level and three dimensional energy based post processing is presented and applied on an actual 90nm product. The preliminary analysis at the package displacement and comparison with measurement maps allow to validade the package model. Then, failure analysis underlines the particular effect of the glue fillet height on the corner die stress features. Hence, thanks to in house energy based criteria, localized evaluation of the crack propagation likelihood into the low-k stack is performed. The particular effects of the glue fillet geometry and die attach thickness are specially studied and combined throught a design of experiment approach. Discussion on failure criteria is also proposed in order to bring inputs on dielectric damaging phenomena in advanced semiconductor products. The sensitivity to shear modes, contrary to compressive one is highlighted, and released energy plots indicate an higher delamination hazard in the bottommost IMD layers. On the other hand a drastic rise of the fracture risk is suspected with highest values of the glue fillet, and thinest die attach.

Acknowledgments

Thanks are due to package experts from Grenoble and Crolles and Toa Payoh ST manufacturing sites.

5.3.2.6

5.3.2.7 References

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5.3.3 3D Multi Scale Modeling of Wire Bonding Induced Peeling in Cu/Low-k Interconnects: Application of an Energy Based Criteria and Correlations with Experiments.

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5.3.3.1 Abstract

Amongst solutions to connect the die to the package, thermosonic wire bonding process remains widely used. However, the introduction of low-k dielectric materials, and the feature size decrease of IC chips to follow Moore's law, pose great integration challenge.

This paper aims to demonstrate the compliance of the proposed modeling approach with the aids of experimental validations. 3D multi scale simulation of both bonding process and wire pull test is carried out. Using a previously validated homogenization procedure to include pad structure description even at the global scale, stress fields acting in the copper/low-k stack are evaluated. The modeling strategy also includes an in-house developed energy based analysis.

For the experimental part, a wide range of wire bond trials have been performed in order to qualify the 65-nm technology node. On behalf of that, several bond pad architectures have been implemented and wire bonded on a test vehicle. It was found a significant effect of the copper/low-k design on peeling failure rates, in particular with severe bonding conditions.

In this paper, typical modeling results are presented. Contrary to stress based one, the energy based analysis shows a better ability to forecast the observed failed interface. From simulation results obtained, it is confirmed that the bonding process plays major role in the peeling failure, despite the fact that most of them are observed during the wire pull test. Failure mechanisms are also proposed. Then, the implemented pad structures are evaluated and analyzed. Both general trends and architecture ranking are provided. Simulations are then faced to experimental results and a full agreement is found. The complementary nature of the energy based failure criteria is again highlighted through a clearer discrimination of the tested structures.

Finally, the simulation procedure with confirmed experimental results demonstrates its ability in design and process optimizations by providing a better understanding of pad peeling failure mechanisms.

5.3.3.2 Introduction

Amongst solutions to connect the die to the package, thermosonic wire bonding process remains widely used. However, the introduction of low-k dielectric materials, and the feature size reduction on IC chips following Moore's law, pose great integration challenge [1]. On one hand, as the k value is reduced by introducing porosity into low-k materials, their mechanical behavior becomes less robust [2]. On the other hand, with the critical dimension reduction, stresses induced by both front-end of line (FEOL) and back-end processes like wire bonding tend to increase [3, 4]. Delamination failure modes are now commonly observed and mechanical integrity of IC has became a key integration issue [4].

Modeling is one of the major tools used to understand and reduce mechanical related defects. Various design concepts can be evaluated early in development, without actual silicon. More precisely, it is observed that the interconnect pad architecture plays a great role in peeling failure rate [6], and finite element modeling has demonstrated its ability to provide insights for bond pad design optimization [7]. However, due to the complexity of the physical phenomena involved, added to very detrimental aspect ratio from die level to interconnect one, specific modeling methodologies need to be developed.

5.3.3.3 Modeling Methodology

Multi scale and homogenization procedure

Typical dimensions involved in wire bonding induced peeling failures have a very wide range: During the wire bonding process, macroscopic and uneven loads are imposed by the gold wire, with bonded ball diameter (BBD) of about 32um and 36um for 40um and 50um bond pad pitch respectively. On the other hand, in the peeling region, i.e. the interconnect levels, very thin layers such as the hard masks

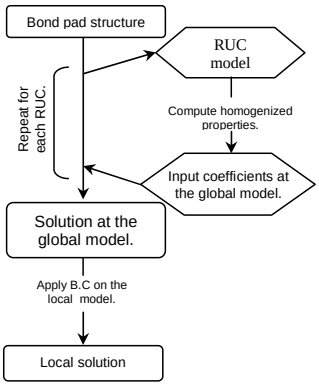


Figure 52 Multi Level and homogenization technique: Flow chart.

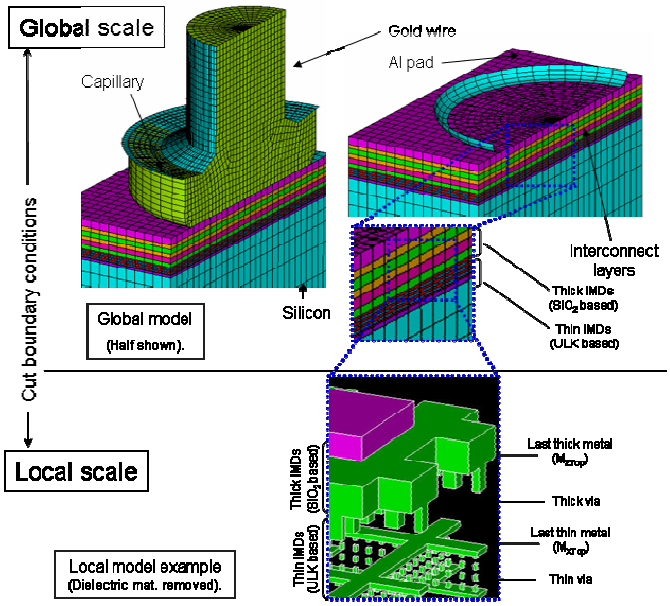


Figure 53 Finite Element Models: Bond pad & wire assembly at the global scale (top) and interconnect structure at the local scale (bottom).

with a typical thickness of 30nm are concerned. Moreover, due to the bond pad architecture, the use of a three dimensional (3D) analysis is mandatory and a common plane strain assumption is not suitable. Indeed, a two dimensional approach has many drawbacks: For example, distinction between via and metal line is not possible, and interconnect patterns such as dielectric enclosure can not be described. Hence, to consider the very detrimental aspect ratio would lead to a huge amount of elements with a single 3D FE approach and multi-level modeling need to be performed.

The main steps of multi level modeling are the following (Figure 52 & Figure 53):

- Compute a first simulation at global level to get displacements field.
- At the global level, locate the maximum strained area, i.e the future location of the micro model.
- Apply the displacement field calculated at the macro level as boundary conditions of the micro model in order to reach the local stress field.

The key point of the multi scale method is to be able to describe the materials and the bond pad layout which compose the macro model with a sufficient amount of details in order to calculate properly the displacement field. At this stage, a homogenization procedure needs to be defined. This accounts for the geometrical details by modifying the mechanical properties without meshing all the

interconnect layers.

Several ways to perform this step can be used. However, it has been shown that precautions must be taken, in particular concerning the choice of the representative unit cell (RUC) and the rheological model to be applied [8]. Thus, the following method is carried out in this work:

One periodic RUC for each interconnect level is chosen. More precisely, the Inter Metal Dielectric (IMD) architecture and the Metal geometry are considered separately and thus for each interconnect level. This leads to a dozen of equivalent property sets (e.g of a six metal levels (ML) interconnect stack). As for the equivalent behavior of the RUCs, considering both the pad structure designs and the material properties to be homogenized [9], a linear orthotropic model ensures both reliable results and computation efficiency. Hence, the set of equivalent properties for each cell is made up of nine coefficients: (i) Young's moduli E_x, E_y, E_z, (ii) Poisson's ratio ν_{xy}, ν_{xz}, ν_{yz}, and (iii) shear moduli G_{xy}, G_{xz}, G_{yz}. The coefficients are calculated by applying simple loading cases on the RUC and then by extracting reaction forces acting on its boundaries. Consequently, the whole IC stack at the global level will be described by hundreds of parameters.

Then, the stand alone evaluated coefficients are included in the global model and the solution is calculated. Finally, degrees of freedom (DOF) are interpolated and applied to the local model, bridging the gap between the scales and providing stress field at the IC level.

Loading conditions

Once the finite elements models are built, suitable loads must be applied. Even though the peeling failures are mostly observed during the wire pull test, it is already known that such failures are inherently caused by the wire bonding process itself, especially with an unoptimized bonding process. Unoptimized bonding parameters will cause micro-cracks in the bond pad structure during bonding [10, 11]. Hence, in a comprehensive modeling analysis, both the bonding and pull test must be considered.

However, thermosonic bonding mechanism is complicated and the physical motion of the capillary and free air ball (FAB) is difficult to be modeled precisely. Some assumptions need to be made, particularly in the aspect of Au-Al intermetallic formation [11, 12], the interaction of this with the bonding parameters [13, 14] and its effects on pad peeling failure rate. Despite the fact that some

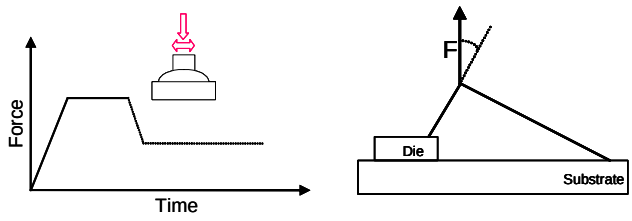


Figure 54 Schematic of the applied loads: Stage 1 (left): Simplified bonding process, in solid lines the simulated step. Stage 2 (right): Wire pull test (right).

technological barriers remain in analyzing the whole mechanism by simulation, some promising works have been published recently proposing various approaches for investigating, although often separately, the various factors of wire bonding physics [3, 15, 16, 17].

In this paper, considering both the requirements for 3D bond pad architecture optimization and the aforementioned limitations, a simplified modeling of the bonding process is proposed, followed by the standard wire pull test simulation (Figure 54): Starting from the bonded ball which has non linear material behavior, both contact and ultrasonic steps are reproduced in a 3D model. The model considers that a rigid capillary carries the wire with a normal force and horizontal displacement resulting from the wire bonding parameters. Whereas the applied pressure value is provided directly by the parameter of bonding machine, the determination of the ultrasonic displacement value is rather subjective as it is not quantitatively controlled once the contact is established with the bond pad surface. The tangible displacement of the capillary can be measured as a function of the 'power' parameter in the wire bonder. In this modeling work, despite the decrease of ultrasonic displacement during the contact stage, it is assumed that the capillary and FAB displacement is consistently following the 'power' value used in the model. In later stage, the capillary is removed from the model and wire pull test at a given angle is performed. The force acting during this load step is extracted from the measured wire strain-stress curves provided by the wire suppliers.

Failure Criteria

Finally, suitable criteria must be defined according to the observed failure modes and by taking into consideration of the material set used. Despite the fact that in-situ investigations of the failure modes are tricky, the most likely scenario in the case of peeling failures is brittle fractures. Furthermore, micro-crack is highly suspected at the early stage of peeling failure, which is initiated at the many interfaces of metal layer and low-k dielectric. Hence, the targeted failure mode, which is brittle delamination, is related to fracture mechanics and specific energy based numeric tools are developed [18, 19]. The so-called Nodal Released Energy (NRE) post processing procedure is based on the computation of energetic quantity from the nodal solution. To evaluate the NRE value, two simulations are required: One with an undamaged model, the other with the damaged one where a virtual crack has been inserted. At this step the crack properties need to be defined: The out of plane locations of the crack is at the weakest interfaces of the model, and the peak stress values are analyzed to put the crack in the suitable region. Figure 55 shows the post processing flow chart and formula.

Note that the numerical parameters to be used, the sensitivity and the ability to link this value with the energy release rate has been previously validated; and additional insights compared to a standard stress based analysis have been demonstrated [18]

5.3.3.4 Finite Element Models

Multi level models

The three dimensional bonding model consists of a silicon die containing the interconnect layers, the gold wire and ball, and the capillary. The simulated die stack is seven copper metal levels (7ML) including five low-k levels and the two others containing classical silicon dioxide dielectric. Above the copper/low-k stack, the oxide passivation and aluminum bond pad are modeled. Dimensions and material properties are those used in advanced products of 65-nm technology, in which ultra porous low-k dielectric is integrated. Figure 53 depicts the two models used in that multi scale simulation, a meshed interconnect unit cell is provided as an example. On the local model, particular care must be taken to prevent (i) mesh dependency, a Manhattan type mesh with a constant element size is used for all the simulated interconnect pad structures; (ii) interpolation error when transferring boundary conditions from global to local where dimensions of the local model are kept constant in all simulations, disregard the periodicity of the pad design.

Simulated bond pad layouts

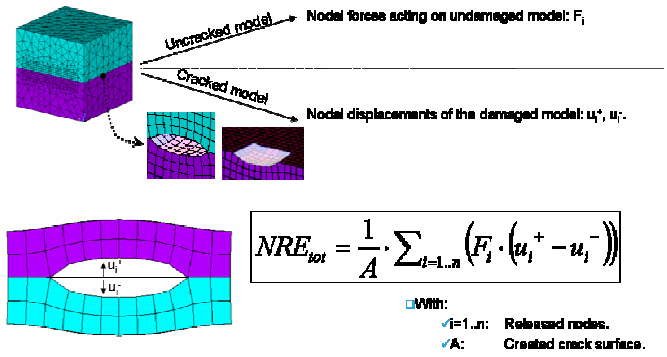


Figure 55 Energy based failure criteria: Nodal Release Energy (NRE), flow chart and formula.

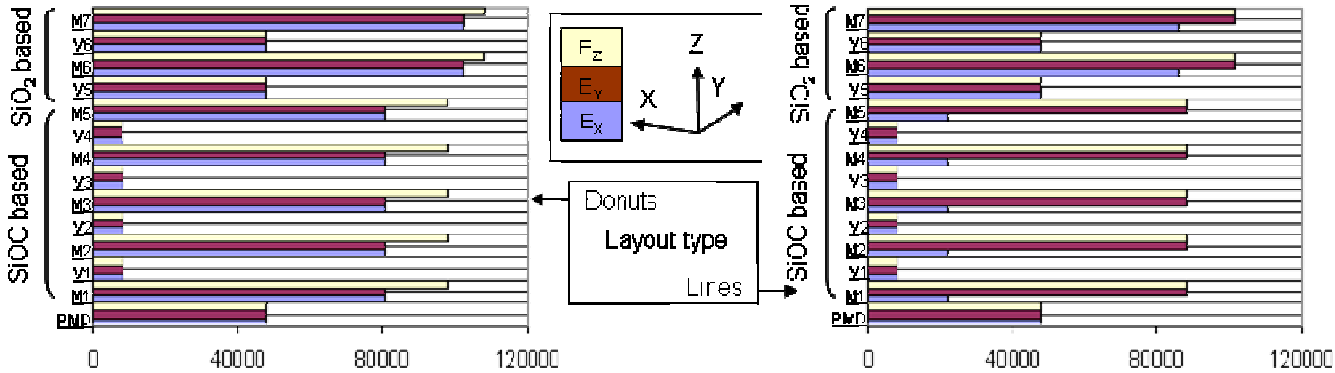


Figure 56 Homogenized properties for the two kinds of metal layouts simulated: Donuts (left) and lines (right). Effective Young's moduli in the three directions and per interconnect layer.

Four bond pad architectures are simulated (Table 4), by varying two parameters:

- Two metal layouts: the one made of metal lines oriented in a single direction, the other made of crossed metal lines. The corresponding structures will be named respectively 'lines' and 'donuts'.
- Two sets of copper space and width: Named respectively 'narrow' and 'wide'.

Note that, for a given metal layout, the equivalent stiffness of the narrow and wide structure are the same, due to the fact that metal density is left unchanged. By consequences, the pad strength would be only affected by local considerations that could not be investigated in the global model.

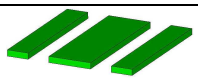
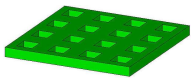
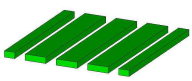
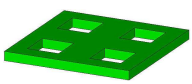
In the frame of the multi level approach, the equivalent properties need to be computed as proposed in 8]. Figure 56 shows the effective Young's modulus of the simulated structures, which is one of the main properties that affect pad strength. Apart from any resistance related consideration, the following differences are observed in the homogenized properties sets: (i) The 'donuts' structures have equal in-plane stiffness (x axis equivalent to y), whereas the 'lines' structures are in plane oriented (x axis not equivalent to y). This could play a role in results, from both experimental and modeling points of view. (ii) Compared from 'donuts' structures, stiffness of low-k layers in 'lines' structures shows an huge decrease in x direction, widthwise (-70%), a slight increase in y direction, lengthwise (+10%) and a slight decrease in vertical direction (-10%).

5.3.3.5 Simulation results

Typical results and failure mechanisms assessment

Prior to any pad structure related consideration, a preliminary study is carried on in order to capture general considerations from the before described simulation method. Both loading steps are performed on standard bond pad architecture and maximum stress locations are determined on the top die surface. More precisely, distinct critical sites are found with respect to the considered step: During the bonding, the maximum stressed area is located just below the capillary tip near the edge of the ball. Whereas, after the wire pull test, peak stress is located below the wire, and it is closer to the central region of the bond pad. These considerations will be used in both global and local levels analysis. Indeed, on one hand the in plane locations of the likely crack nucleation sites are defined and NRE can be computed at the global scale. On the other hand, the degrees of freedom (DOF) calculated at the boundaries of these regions will be interpolated to be applied in the local interconnect models.

TABLE 4: SIMULATED PAD STRUCTURES

PAD #	LOCAL MODEL (COPPER MAT. ONLY)	PATTERN SIZE	METAL LAYOUT TYPE
A		WIDE	LINES
B		NARROW	DONUTS
C		NARROW	LINES
D		WIDE	DONUTS

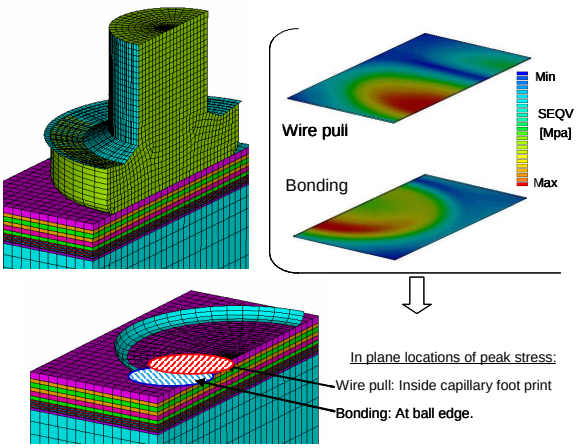


Figure 57 Locations of the peak stresses during bonding process and wire pull test, corresponding to the evaluation sites for energy released quantity.

Thus, the NRE is evaluated at each low-k interface at the vertical points of the stress extrema (Figure 57). The corresponding NRE values are plotted on Figure 60 separately for bonding and wire pull processes. Opening modes are split into a peeling or crushing component (mode I), and a shear one (mode II/III). Hence, for the considered bonding parameters, pull test angle and force magnitude, results are analyzed as follows:

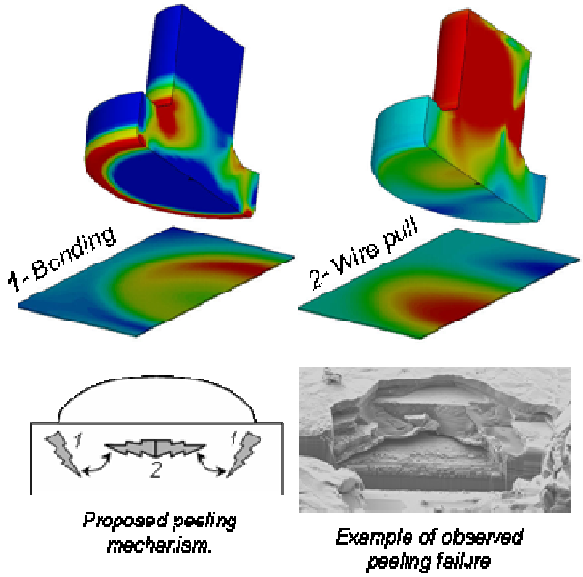


Figure 58: Peeling mechanism assessment (bottom left) from stress analysis during bonding (top left) and wire pull (top right). Bottom right: Post mortem picture of a peeling failure example observed after pull test.

-
- The opening mode I is the most dominant for both loading conditions, i.e. during bonding and wire pull test. On the other hand, the mode mixity is found quite constant throughout the different IMD interfaces.
- The maximum NRE value is found in the top region of the interconnect, but not at the uppermost interface. It must be noticed that, contrary to stress values which show a continuous decrease from die top to substrate 18], the maximum energy based quantity is found inside the stack. This suggests that the main delamination path would not be located at the highest low-k interface, but slightly beneath. This feature is in good accordance with experimental observations (Figure 59) and underlines the relevance of the NRE.
- NRE values computed for bonding process are about two times higher than those for pull test. This confirms our perception that despite most peeling failures are observed during wire pull test, interconnect underneath bond pad could have probably been damaged in the early wire bonding process.

From these results, assessment for the peeling failure is proposed: During bonding, the delamination would nucleate first in a circular pattern around the edge of the bonded ball. Since tensile stress state remains limited during this step, the integrity of the pad is not altered, and cracks are only initiated. Then, the traction load induced during the wire pull test would create another nucleation site concentrated in the centre of the bond pad. Finally, both nucleation sites would merge and lead to the complete delamination of the interconnect levels. In addition to the stress and energy based analyzes, the experimental horseshoe shaped of the fracture path would support this scenario (Figure 58).

Pad structures comparison

In this chapter, the strength of the four pad structures previously described are compared by the mean of the proposed simulation method. Since some of the pad structures show similar homogenized properties, its discrimination at the global scale is not feasible. By consequence, the whole macro/micro process, including discretization of the interconnect copper patterns need to be carried out. Then, from the local solution, stress and energy based criterion are applied to investigate peeling hazard and then bring insights for pad selection and conception.

Stress based analysis

To reach the precise stress state in the interconnect layers, simulations at the global scale are performed with the suitable set of homogenized properties calculated according to the four bond pad structures. Then, the DOF calculated at the global scale are interpolated near the maximum stressed region of the bond pad according to conclusions previously exposed, and thus for the two loading conditions. Hence, considering an ILD layer at the middle of the copper/low-k stack, stress fields inside the four pad architecture can be compared. Stress maps presented in Table 5 show figures in the low-k material for a given interconnect level of the four simulated structures. For comparative purpose with respect to the pad structures, the color map is kept unchanged for a given load and stress component.

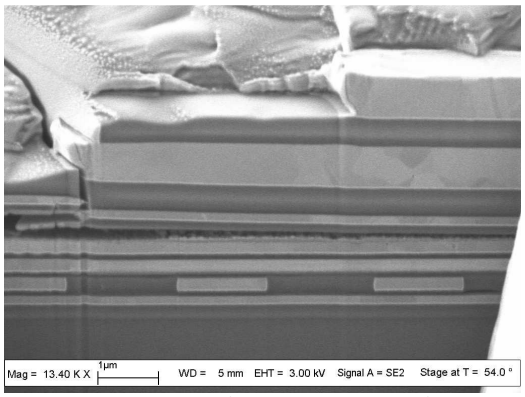


Figure 59 FIB cross section after pull test: Typical fracture path for peeling .failure, delamination located at the upper part of the low-k stack (courtesy of C2A Charac. team).

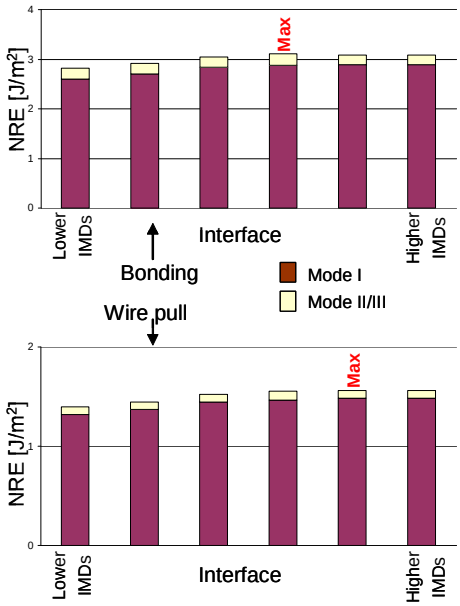
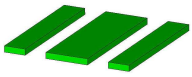
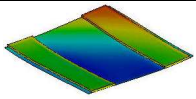
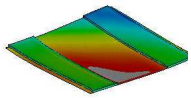
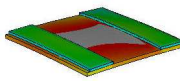
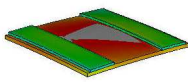
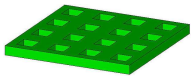
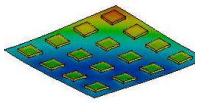
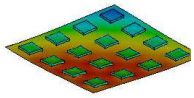
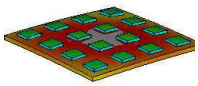
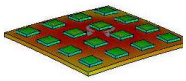
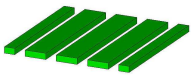
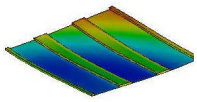
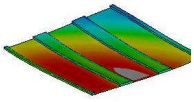
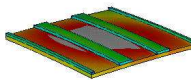
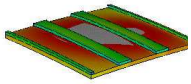
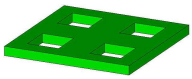
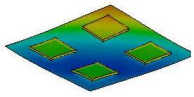
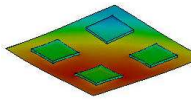
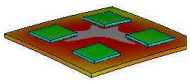
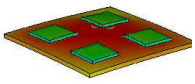


Figure 60 NRE results at interfaces for bonding process (top) and wire pull test (bottom).

TABLE 5: LOCAL LEVEL ANALYSIS: STRESS BASED

				BONDING		WIRE PULL	
			STRESS COMPONENT →	3RD PRINCIPAL	VON MISES	1ST PRINCIPAL	VON MISES
PAD #	LOCAL MODEL (COPPER MAT. ONLY)	PATTERN SIZE	METAL LAYOUT	Min Max			
A		WIDE	LINES				
B		NARROW	DONUTS				
C		NARROW	LINES				
D		WIDE	DONUTS				

Based on these results, it can be seen that: (i) Maximum stress values are found just below the copper patterning contrary to the plain dielectric regions of the cells, which are less constrained. (ii) Differences from structures remain limited and discrimination is not obvious. Consequently, it should be accepted that a stress based analysis is not sufficient to draw conclusion on the metal layout and patterning effects of the simulated bond pads.

Energy based analysis

To apply the energy based post processing method, two cracks which have distinct initial lengths are introduced in the local model, as defined above. These virtual cracks are inserted at the middle of the copper/low-k stack in the maximum stressed region of each unit cell.

a) Architecture ranking

The released energies are presented in Figure 62. Consistent trends are found as the analysis values suggest very obvious conclusions. It is found that the best structure, i.e. the one for which the NRE value is the lowest, is the 'wide donuts'. The 'narrow lines' patterning is expected to be the worst one. As for the two other structures, the difference is insignificant as the results are roughly the same from some of the runs. However, it seems that in the bonding step simulation, the 'narrow donuts' performs slightly better than 'wide lines'. Hence, the energy based analysis suggests the following ranking, starting from the best structure to the worst one: 1- Pad #D, 'wide donuts'; 2- Pad #B, 'narrow donuts'; 3- Pad #A, 'wide lines'; 4- Pad #C, 'narrow lines'.

b) 'Narrow' vs. 'wide' pattern size

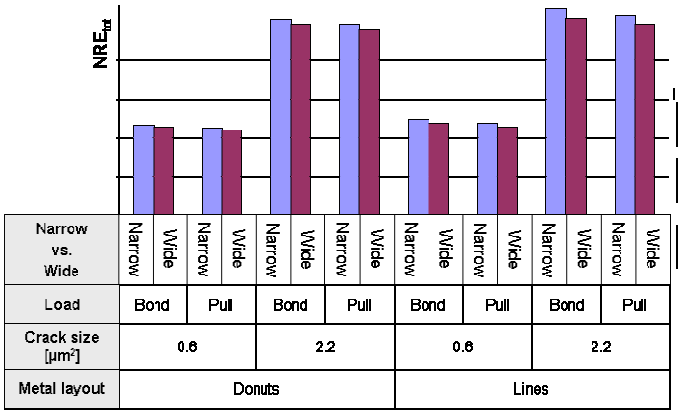


Figure 61:. Energy released for both loads, two crack sizes and the four simulated bond pad structures. Investigations of the pattern size effect.

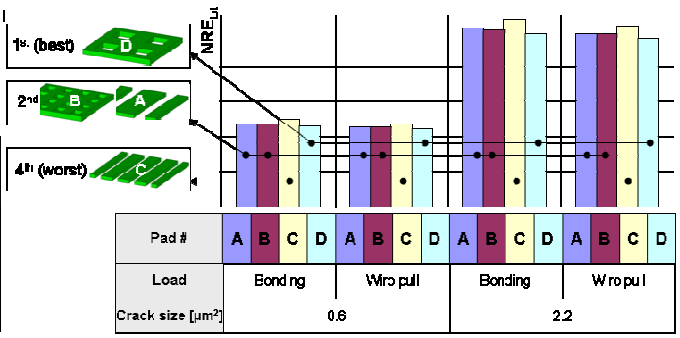


Figure 62: Energy released for both loads, two crack sizes and the four simulated bond pad structures.

In order to separately investigate the effect of the pattern size, the NRE values are presented differently in Figure 61. It shows clearly that for the simulated structures, 'wide' structure behaves better than the 'narrow' ones. Then, for the considered architectures and apart from any metal layout consideration, enlarged metal slotting gives better peeling strength.

5.3.3.6 Experimental correlation

Test procedure

In order to qualify a technology node, a wide range of wire bond trials are performed and various wire bond responses are collected. One of the important response in wire bond is the wire pull test. The test procedure consists of the following steps: First wire bonding operation is carried out, followed by a wire pull test, then a visual visual inspection on the bond pad is performed to determine the the pull test failure mode and to check the integrity of the bond. Finally, categorization of the results in order to provide a reliable statistical data and rates are obtained with respect to each failure mode: Wire neck break, non-sticking corresponding to intermetallic issue, or peeling with delamination at die level. Neck break failure mode is expected if the bond pad and bond interface remains in good integrity. During product qualification, only the neck break failure mode is being accepted.

Experimental DOE and correlations with modeling

In the frame of 65-nm node qualification, several factors are studied on a test vehicle, including material changes, wire types and bonding parameters. The simulated structures are implemented on the die and, at the early stage of the process optimization, a significant rate of peeling failures is encountered. It has been also found that peeling amount was highly dependent on the pad architecture. Note that unfortunately, only three over the four simulated structures were tested, with

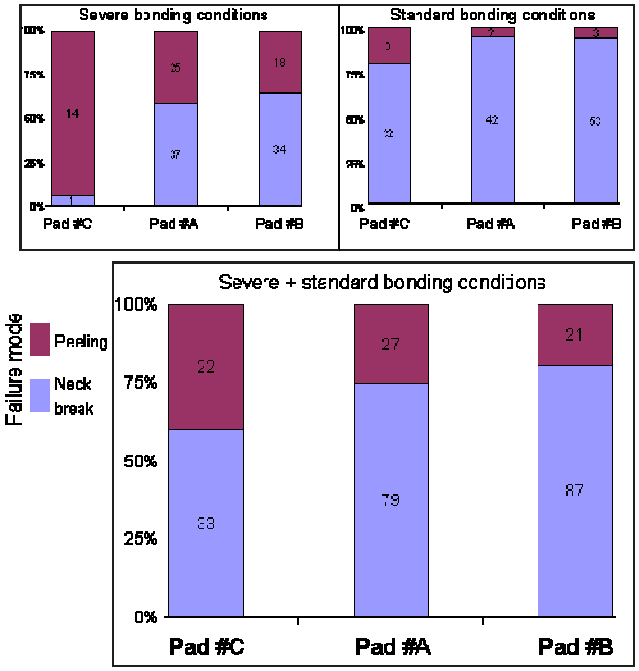


Figure 63:.Experimental peeling rates for the three tested structures and two bonding conditions: Severe bonding parameters (top left), standard (top right), and summed data (bottom).

the pad D (i.e. 'wide donuts') not tested. Despite the fact that only partial experimental data is obtained compared to full comparison results from modeling, there is a clear trends seen in the pad peeling result on different pad structures. Figure 63 summarizes peeling rate for the three tested architectures with two bonding parameter sets.

From the presented experimental results, conclusions can be stated and comparison with the numerical simulations is hereafter carried out:

(i) The 'narrow lines' structure (Pad #C) shows the highest peeling rate. This is confirmed by the ranking established from simulation depicted in Figure 62.

(ii) Depending on the bonding process, discrimination between Pad A and B is not obvious. However with severe bonding conditions, the 'narrow donuts' pad B behaves better than the two others, whereas for standard bonding process, pads A and B show similar strength. This is also in agreement with simulation (see Figure 62). Indeed, it suggests that, only for the bonding load, a slight variation of the NRE is observed from these two pads showing a higher strength for the 'narrow donuts' (Pad B).

5.3.3.7 Conclusions

In order to evaluate IC architectures with respect to wire bonding induced peeling failures, 3D multi scale simulations of both bonding process and wire pull test have been completed. Using a previously validated homogenization procedure to include pad structure description even at the global scale, stress fields acting in the copper/low-k stack have been evaluated. The modeling strategy includes two kinds of analysis, a stress based one and an energy based one. The latter founded on a propagation approach, as suggested by the observed failure mode.

During the 65-nm technology node development, a wide experimental DOE provided reliable statistical data, which has been used in this work for correlation purpose. The effect of the bond pad structure on the peeling failure rate has been particularly studied. Modeling results have been found to be fully in agreement with experiments, and additional insights, particularly on the suspected creation of the delamination phenomena, have also been proposed.

Furthermore, the complementary nature of the energy based failure criteria has been highlighted through a clear discrimination of the tested structures. In addition, the effect of the pattern sizing for similar layouts has been identified at the local modeling level.

Finally, the simulation procedure with confirmed experimental results demonstrates its ability in design and process optimizations by providing a better understanding of pad peeling failure mechanisms.

Acknowledgments

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5.3.3.8 References

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5.3.4 Advanced Reliability Modeling of Cu/low-k Interconnection in FCBGA Package

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5.3.4.1 Abstract

Thermo-mechanical simulation is carried out on the Cu/low-k FCBGA (Flip-chip Ball Grid Array) package for high performance server applications. Global-local modeling methodology is performed. Layered structures for both build-up substrate and Cu/low-k layers are established. The build-up substrate is divided into inner and outer areas based on the Cu distribution, and equivalent properties for each area are obtained. A homogenization method which enables to take exact Cu/low-K layout into account is developed to obtain the equivalent properties of interconnects. Furthermore, faithful simulation of the consecutive material deposit steps has been performed in order to reproduce the whole fabrication process. Stress state induced by both front-end and packaging processes has been studied based on the established methodology. Thus, potential sites for delamination are identified. For critical sites, fracture mechanics approach is applied, and energy release rate is computed in order to determine the reliability of copper/low-k interconnects. Delamination hazard is investigated in several areas of the interconnects, and discussions are carried out concerning crack propagation phenomena.

5.3.4.2 Introduction

As the feature size of IC chip is decreasing continuously to follow Moore's law, Cu/low-k or ultra low-k interconnection is becoming a mainstream for high performance ICs. The low-k or ultra-low-k materials are more brittle than conventional dielectric [1], which creates great challenges for packaging and assembly. Packaging can significantly impact wafer-level reliability, e.g. interfacial delamination in Cu/low-k or ultra low-k interconnects during packaging process can occur.

Amongst packaging solutions, flip-chip assembly induces high stresses to interconnect layers through the bumps. Indeed, a large coefficient of thermal expansion (CTE) mismatch between the silicon die and the package produces device bending which must be borne by the active part of the flipped die. Such interactions have been previously investigated [2-3-4]. Results confirm that the package leads to high stresses at interconnect levels. Parametric studies have also been carried out and main influencing factors have been highlighted. More precisely, package geometry and type, material properties and initial stress effect have been particularly studied.

In this paper, a 2D plane strain multi-level simulation is conducted aiming at evaluating precisely the stress state in the device. In order to reach this goal, both interconnect process induced stress and packaging stress due to the underfill cooling of a flip-chip package are considered. This study particularly focuses on the interconnect level.

First of all, the modeling methodology is described and failure criteria are discussed. Both stress and energy based analyses are performed and compared. Due to their weak adhesion properties [3], interfaces between the low-k material and the metal barrier are closely investigated. Finally, a discussion related to the crack propagation hazard at several locations of the interconnect stack is put forward.

5.3.4.3 Modeling Methodology

Level Submodeling and Homogenization Procedure

Since the packaging will have a great impact on the Cu/low-k interconnection, reliability study on the FCBGA package will span from package level (package dimension: 45mm x 45 mm) to interconnection level of a CMOS90 device. The dimension ratio is about 1/500,000. It is impossible to use a single finite element model to simulate the detail of the interconnection features without a super-computer. Fortunately, sub-modeling techniques can be used to deal with this kind of problem with less computation effort.

The concept of sub-modeling is to build two models. The first one is a global model with relatively coarse mesh pertaining to the global boundary conditions (BC). The second one is called a sub-model, containing a detailed mesh for the specific area of interest. The sub-model's BC is inherited from the global model by interpolating the nodal displacements and body forces from the global model. The accuracy of the sub-model is dependent on the coarseness of the global model and the details of the sub-model. For the current FCBGA model, one level of sub-modeling is not enough due to the huge dimension span. Thus, multi-level sub-modeling is required, i.e. a second level (or even more) local model is nested in the first level local model. In the first level local model, Cu/low-K interconnect layers are modeled as simple equivalent materials.

One of the key points of the multi-level modeling technique is the evaluation of the equivalent properties of the materials. Among the required steps, the choice of the representative unit cell (RUC) used for the homogenization is of the utmost importance. . Indeed, depending on the RUC, an inaccurate evaluation of global level displacements may occur, leading to errors in the local level calculated stress and strain fields. The complete homogenization procedure used for the interconnect layers was previously described [5]. More precisely, it is shown that a simple volume averaging is unable to render the anisotropic behavior of the interconnects and that a discretization of the Inter Metal Dielectric (IMD) layers added with orthotropical equivalent material properties are mandatory.

Fracture Mechanics

Compared to classical stress based criteria, the fracture mechanics approach is the most suitable way to address failure mechanisms and to quantitatively evaluate semiconductor architectures [2, 6]. A wide part of the failure criteria investigated in this paper is dedicated to the fracture mechanics approach. More precisely, the total energy release rate (ERR) is evaluated in some particular interconnect areas aiming at quantifying the crack propagation hazard. Nevertheless, this approach's limitations need to be detailed. The main assumptions and restrictions are the following:

- Only the propagation phenomena is quantified. Indeed, an initial defect must be introduced and the ERR value is then computed given this defect. The calculated G value is finally compared to a critical value G_c. This enables to forecast either crack stability or crack growth according to Griffith theory. As a result, the nucleation phenomena, for which no widely accepted formalism is known, is not addressed with such an energy based criterion.
- Moreover, in the particular case of adhesive crack, which is the main failure mode in interconnects [1], another rising issue is to be able to define the critical G value G_c. Indeed, the G_c value is strongly dependant of the mode mixity and experimental G values under mixed mode conditions which are hardly measurable [2, 7]. However, a comparison of the calculated G with the critical value in the first propagation mode enables a safe estimation of the propagation hazard.
- Despite the initial defect size, assumptions are also made concerning the crack shape and direction of propagation. It is assumed that the crack propagation is aligned in the initial crack direction, and no kinking of the crack is allowed. Note that this assumption could be strong for cohesive fractures. In the case of a delamination phenomena however, it is likely that the crack propagates along the interface, due to the fact that the interface strength is generally weaker than the cohesive strength.

Considering these limitations, there are many numerical techniques to compute the ERR from a finite element solution. One of them is particularly attractive and adapted to brittle materials: the Virtual Crack Closure Technique (VCCT) [8-9] which seems to be efficient. Indeed, this method does not need a specific mesh, and the postprocessed variables are directly available from a standard FE solution. The total G value is defined as the addition of each G_i components related to the direction considered. To compute each G_i component, ERR value can be extracted from one of the two crack tips, using the following equation:

$$G_i = \frac{1}{2\Delta a}\left[F_i \cdot \left(u_i^{+} - u_i^{-}\right)\right] \qquad (1)$$

where Δa is the considered crack extension (i.e. the element size at the crack tip), F the nodal force acting on the crack tip node and u the displacements of the first opened node.

Moreover, in order to reduce the CPU time when a high amount of crack configurations need to be tested, a multi level technique has been developed and used in this study in addition to the VCCT. This enables to run a single solving operation of the undamaged model, and then to solve a reduced amount of elements for each crack location. A preliminary work consisted of testing and validating this approach on some simple cases where the analytical solution is known. Results show that, with a

sufficient mesh refinement of the crack tip, a very good agreement is found between analytical and FEM solutions for various configurations and load cases.

FEM Model

The FCBGA package (see Figure 1) consists of the silicon die, solder bumps, underfill encapsulant and BT substrate. A copper cover lid is attached on the top of die and substrate by a thermal interface material (TIM).

A 2D plane strain model is established, and only ½ of the package is modeled thanks to symmetry. A three-level sub-modeling strategy including a global model, first level local model (#1) and second level local model (#2) is used, as shown in Figure 2. The global model is the whole flip-chip package model including the die, underfill (UF), built-up substrate, Cu lid and stiffener, and solder bumps. The mesh of the global model is too dense to show the element outlines. The local model #1 includes only a portion of the package containing the die edge and the outermost solder bump. It uses the displacement generated by the global model as boundary conditions (cut boundary). The Cu/low-k interconnections are homogenized into different layers with equivalent properties, which will be described later. The material properties are listed in Table 1.

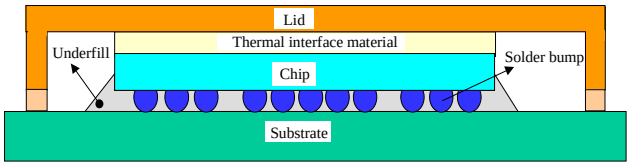


Figure 1. Diagram of FCBGA package

The substrate for the FCBGA is a built-up multi-layer structure to save space (see Figure 3). Because Cu is not evenly distributed in each layer of the substrate, the built-up substrate is divided into inner and outer regions based on the Cu distribution (as shown in Figure 4), and equivalent properties for each unit are obtained by averaging.

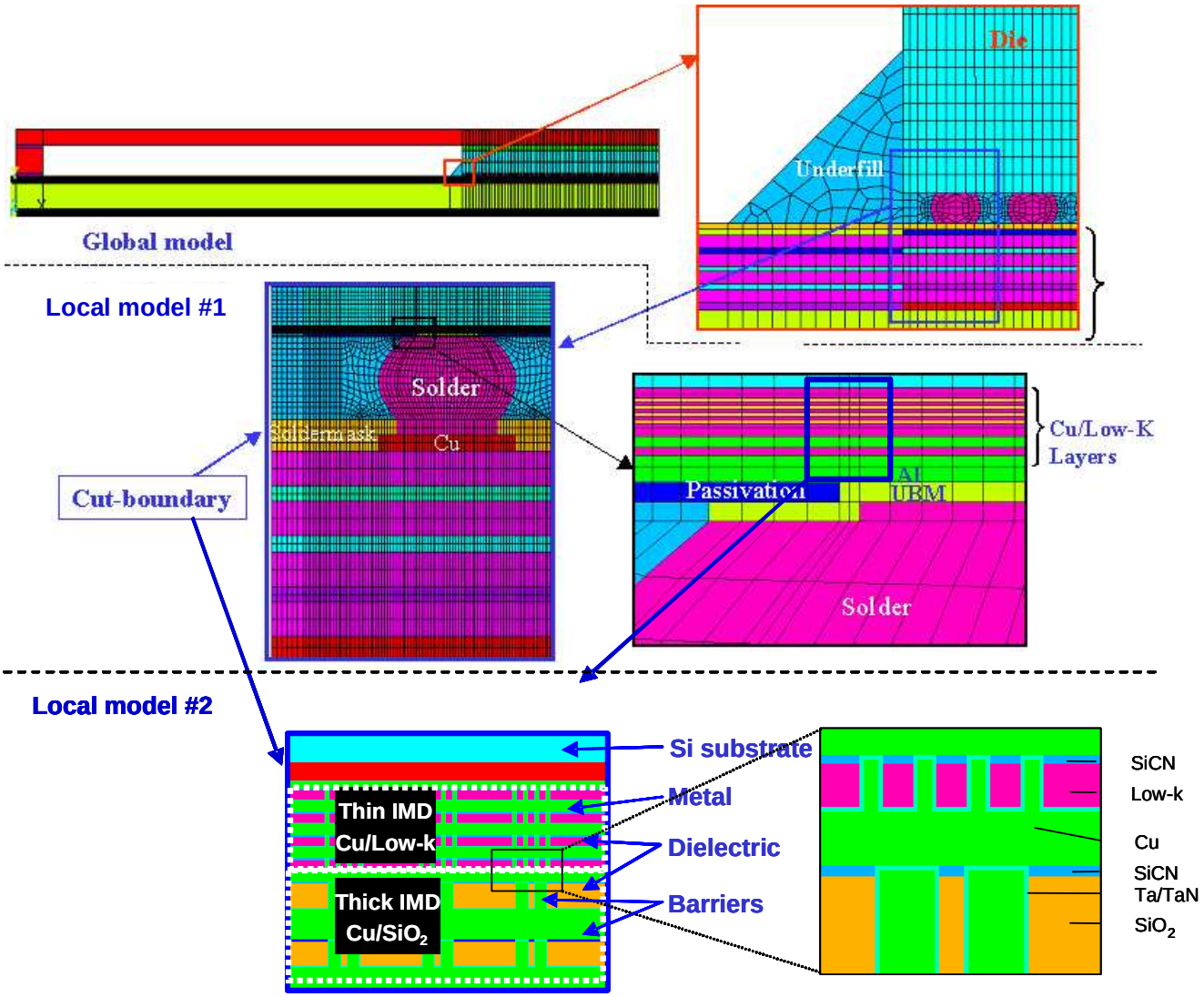


Figure 2. Three-level sub-modeling of Cu/low-k in FCBGA

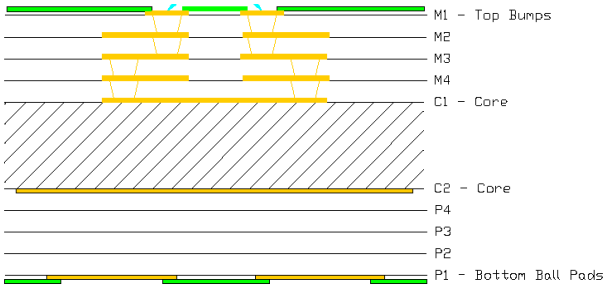


Figure 3. Diagram of built-up substrate

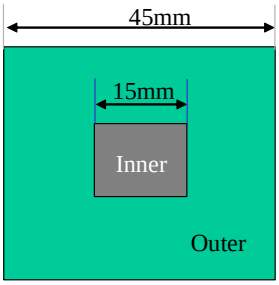


Figure 4. Separation of substrate based on Cu content

Table 6. Material properties of package models

Materials	CTE1 (ppm/^{0}C)	CTE2 (ppm/^{0}C)	Tg (^{0}C)	E 1 (GPa)	E 2 (GPa)
Silicon Die	2.8	-	-	131	-
Copper	17.4	-	-	127.4	-
Aluminum	23.6	-	-	70.5	-
UBM	130.9	-	-	130.9	-
Passivation	3 / 52	-	-	200 / 2.9	-
Solder Bump	25	-	-	31.6	-
Rim Adhesive	39	162	49	4	0.107
Underfill	35	100	75	10	0.05
TIM	-	189	-121	-	0.013
Substrate Core	X:13/Y:15/Z:30	-	165	25	-
Build-up Dielectric	47	155	177	4.0	-
Solder Mask	60	160	104	2.7	-

Figure 2 shows the finite element model of the interconnects. The simulated device is a 7M2T product, i.e. a so-called front-end structure with five metal levels having low-k dielectric, and two other thick levels having standard SiO_2 material as insulator. This stack is typically used in advanced applications. The simulated periodical pattern corresponds to a standard pad architecture for flip-chip and wire-bonding connections. More precisely, the metal layers are made with long copper lines and some vias assume the connection between the metal levels.

As discussed previously, the homogenized properties are computed for each IMD layer and included into local model #1. Results are summarized in Table 2.

Table 2. Equivalent properties of the interconnect layers

Layer name	EX [GPa]	EY [GPa]	GXY [GPa]	AlphaX [*1E-6]	AlphaY [*1E-6]	NuXY
PMD	60.00	60.00	24.00	2.67	2.67	0.25
Thin metal	127.05	127.00	47.74	15.46	15.38	0.33
Via thin	24.70	30.16	4.96	8.62	14.52	0.10
Thick metal	60.40	68.82	22.55	5.24	8.48	0.26
Via Thick	127.82	127.81	48.05	16.38	16.37	0.33

Loading conditions

During interconnect layer build ups, high temperatures are involved and CTE mismatch induces high amount of local stresses. Furthermore, it is well known that the final stress and strain fields depend on the whole process flow and that a single thermal cooling down is not sufficient to calculate process induced stress [10, 11]. Indeed, on one hand the stress free temperature of each material is distinct, on the other hand the interconnect process consists in a successive deposit steps. Hence, aiming to perform a reliable stress evaluation, all the process steps must be considered. Thanks to the use of the so-called birth and death Ansys® option, this can be achieved and the process flow can be reproduced.

Figure 5 depicts the dual damascene process, including nitride and diffusion barriers. These steps are repeated for each IMD level.

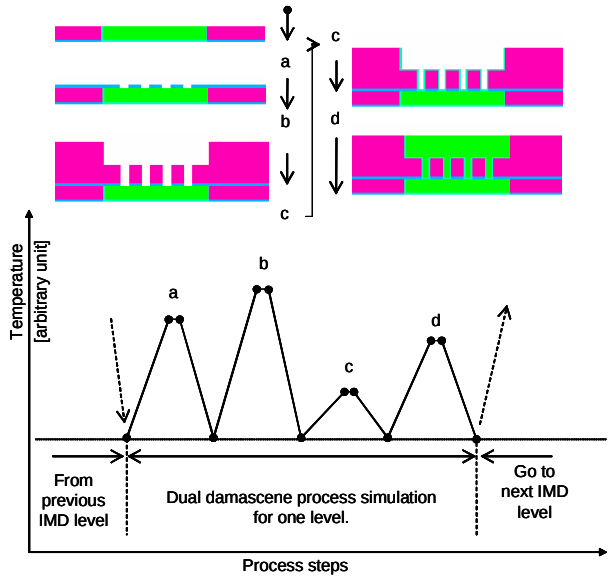


Figure 5 Simulation of the dual damascene process. Ex. for a given IMD layer. Step a: Nitride barrier. Step b: Dielectric. Step c: Ta/TaN barrier. Step d: Copper.

Then, the packaging loading condition is considered and a cooling from 150°C to 25°C is applied on the whole flip chip device. 150°C, which is the curing temperature of both underfill and lid attach materials, is set as stress-free temperature.

Finally, under linear elastic assumption, both stress contributors (i.e. the process induced stress and the packaging stress) are added in the local interconnect model and the final stress state is obtained.

5.3.4.4 Results and Discussions

Figure 6 shows the warpage pattern of FCBGA after Cu lid attach process. It can be seen that the middle of the package warps downward (crying face), while the outer part of package becomes flat. This complex behavior is due to the thermal mismatches between Si chip/substrate, Si chip/Cu lid, and substrate/Cu lid, and their interactions.

Figure 7 shows the stress obtained from global model. It indicates that the maximum stress in die is located at the bottom corner of die, and that the maximum stress in solder bumps is located at the top right corner of the outermost bump, while all four corners are loaded with high stresses.

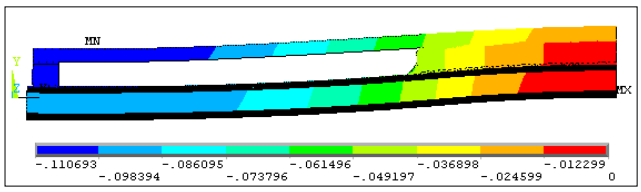
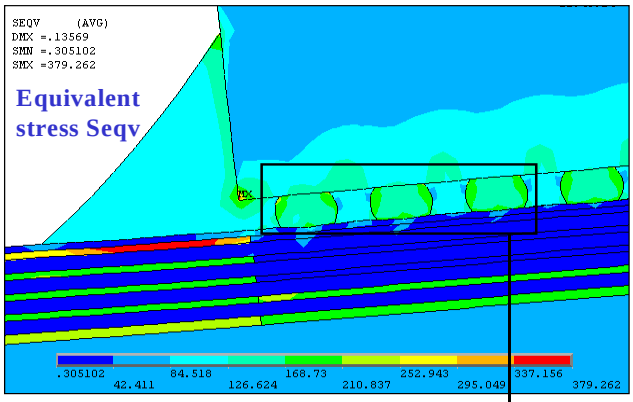
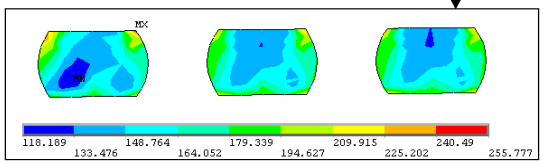


Figure 6. Warpage of whole package along middle-plane cross-section after curing (half model shown)



(a) Stress around die edge



(b) Stress in solder bump

Figure 7. Stress distribution from global model

Identification of Area of Interest at Bump Level

As discussed previously, the very detrimental aspect ratio between the considered modeling levels does not allow description of the interconnect details at the upper modeling levels. However, the global behavior of the front-end patterns is reproduced faithfully, owing to the equivalent properties attribution at the bump level. Therefore, the average solution at the bump level corresponds to the average solution at the interconnect level. Furthermore, in order to evaluate the most critical stress and strain values in the interconnect materials, the area of interest (AOI) must be defined at bump level. These AOI will be the locations of the interpolated boundary conditions at the last level of submodeling. The potential AOI are depicted in Figure 8.

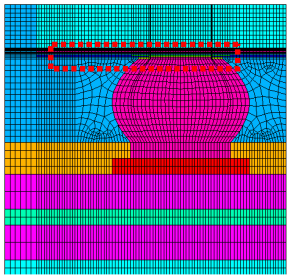


Figure 8. Bump model and potential areas of interest in the interconnect layers (in red).

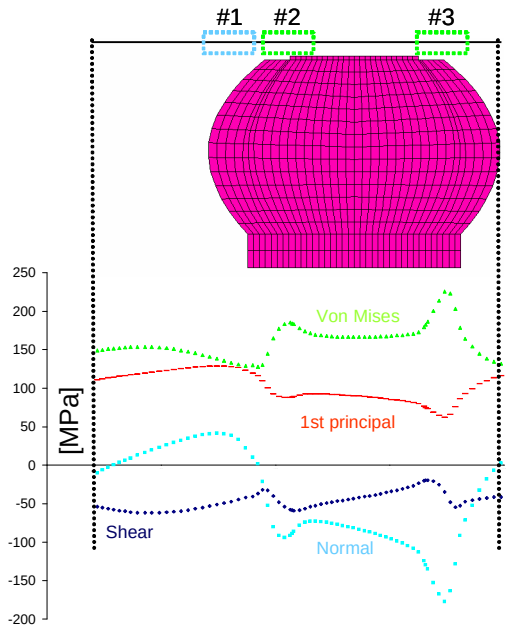


Figure 9. Stress plots to define locations of the cut boundary conditions for the interconnect models. Three potential failure sites are found named #1, #2 and #3. Stress components are evaluated at the middle of the front-end stack

Thus, from the stress and strain fields at bump level, a criterion must be chosen in order to define the AOI. An analysis of the stress components along a path of the interconnect parts of the bump levels provides these insights. Figure 9 shows several stress components: the normal stress to the metal layers, the Von Mises equivalent stress, the planar shear stress and finally the first principal stress component are plotted. Specific failure mode can be attributed to each stress component and peak stress locations must be considered as potential delamination sites at the interconnect level.

At this step, one can wonder which stress component should drive the definition of the AOI. In other words, which failure criteria must be used at the bump level in order to locate the failure sites at the interconnect level. Furthermore, the location of the peak level is different according to the considered stress component.

Three potential failure sites are found in the interconnects considering these stress plots. The first one (named #1 and shown above) is the projected left edge of the bump and corresponds to the maximum normal and first principal stress. The two others (named #2 and #3) are located respectively at the left and right corners of the bump, where Von Mises and shear stresses are concentrated. Another solution to deal with the question of criteria to use would be to evaluate the ERR as defined in the previous paragraph. The advantage of this criterion would be to base the comparison of the potential AOI on one quantified value only (here is the total ERR, *G*). However, the issue of dealing with the observed compressive normal stress between the interconnect layers can be discussed. More precisely, can the behavior of a crack under a compressive loading be treated in the same manner as for tensile state?

Hence, the choice is made to consider several stress components, to find out locations of the interpolated models, and finally apply a stress or energy based failure criteria at the interconnect level.

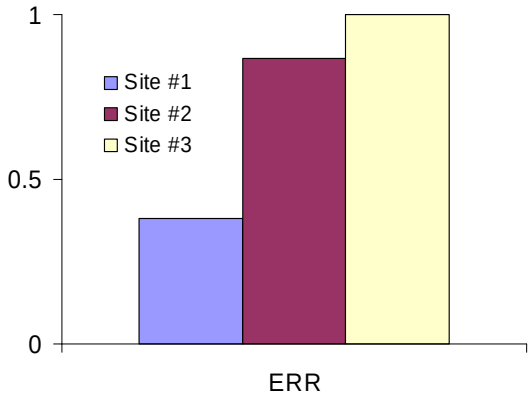


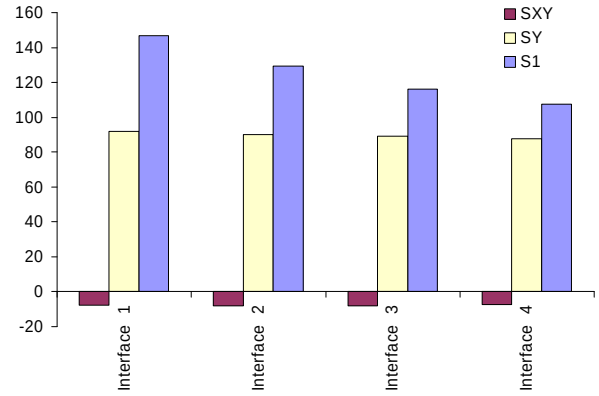
Figure 10 Normalized Energy release rate values compared for 3 potential critical sites at the bump level.

Results of this step have been previously detailed in [4]: The top right bump corner is found to be the most critical site. The analysis also highlights that the same trends are provided by stress and energy based failure criteria.

Plot on Figure 10 depicts the main results and shows ERR calculations for a particular copper/low-k interface.

Considering these results and in order to perform the interconnect level analysis, the next parts of this paper will focus on site #3. More precisely, the established multi scale methodology is conducted at the global package level, then at the outermost bump and finally at the area above the top right corner of the aforementioned bump.

Failure Analysis at Interconnect Level



Stress based analysis: Critical interface

Once the locations of the sub models are defined, the packaging stress can be evaluated. In addition, a full process modeling is performed and quantification of the interconnect process induced stress is provided. Hence, the final stress state at the end of the whole device fabrication steps is obtained.

As measured and reported in [3], the interface having the weakest adhesion strength in low-k structures is the one between the copper diffusion barrier and the dielectric material. Furthermore, post mortem observations of failed structures show fractures with planar paths. Therefore, these interfaces are going to be closely analyzed in the next parts of this study. As for the failure criteria, in case of the use of a stress based one is chosen, which is the most convenient, the component to be analyzed must be previously defined. Based on the assumption of a mode I delamination event, a particular attention is paid at the normal stress component.

Figure 11 shows averaged final stress components calculated at several barrier/dielectric interfaces of the interconnects. A tensile normal stress acts on these interfaces, whereas shear stress value remains low. Results also highlight that averaged stress components are decreasing from the lower to the upper layers.

Stress history

In addition to the final one, the evolution of the stress state during the whole process flow can also be studied. Figure 12 shows the stress history for two particular sites of the first interface as previously defined. Both are situated at the same interconnect level, but at different areas of the architecture in order to point out layout effects: One is located at the vicinity of a via (point A), the other far from a via region (point B).

Nodal stress components are plotted in figure 12, the first principal, normal and shear stress components evolution are depicted. From this curve, common trends can be drawn:

During interconnect build ups, the first principal stress is cumulated, whereas change in shear stress value as a function of time remains low. Changes in the first principal stress value are attributed to the planar stress component. Indeed, during consecutive material deposits, CTE mismatches lead to a stress accumulation that can be compared to a 'sandwich effect'. This effect also points out the need to perform a full process simulation on order to faithfully describe the final stress state.

On the other hand, the packaging step influences differently the stress state and distinct evolutions according to the considered node can be noticed. Indeed, despite the fact that, for the analyzed cases, shear and normal tensile stresses increase during the underfill cooling, the contribution of the packaging loading on planar stress component depends on the local geometry. This shows complex interactions between front-end and back-end features, and local effects of the interconnect architecture.

Energy based analysis

In addition to the above stress based analysis, the application of fracture mechanics methodology is mandatory, as underlined at the beginning of this paper. Since local effects have been previously pointed out, the two interconnect regions are analyzed by the means of energy release rate computations. More precisely, based on the whole process flow, crack propagation hazard is evaluated. A crack length of 0.6µm is arbitrarily chosen and introduced between the weakest interface, i.e. the metal barrier layer and the dielectric, and at various locations of the model.

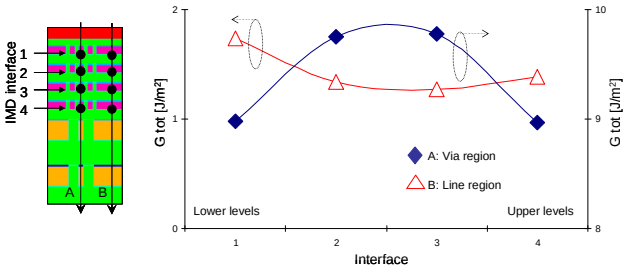


Figure 13 Energy release rate values as a function of the interconnect levels.

Figure 13 shows the energy release rate values at the two aforementioned regions and for all IMD layers of the stack. It confirms that the local architecture plays a great role in the results, and that G values are quite heterogeneous within the interconnect stack: First of all, the ERR values calculated in the via region (path A) are much higher than the ones in the line region (path B). Moreover, the evolution of the ERR according to the IMD layer is reversed for these two points. Indeed, maximum values are found at the top and bottom layers for points A and at the middle of the stack for points B. From this plot, the weakest region regarding delamination issue is found to be at the vicinity of the vias, and in the middle of the low-k stack. However, despite the fact that the contribution of all the stress components is here gathered in a single quantity by the use of energy based failure criteria, to decide on the propagation hazard remains unclear and subject to discussion. Indeed, points A are surrounded by metal patterns and one can imagine that a short crack, which could, according to the calculated G values, nucleate and propagate, would be stopped by metal lines and would not lead the device to electrical failure. On the other hand, since ERR values in the bottom part of the stack and for point B are quite similar to the critical ones measured, it is likely that a nucleated crack would propagate more easily in this region.

Trying to gain an insight into the previous assumption, the evolution of released energy as a function of crack length is investigated. Figure 14 shows the ERR values for several crack lengths. Results highlight that the G value generally increases with the crack length. However, an unexpected

slope change occurs for crack length high values in the point near the via region. Such extrema in released energy values can be analyzed as a stable point. More precisely, at this inflection point, the system would not release some additional energy by the mean of crack propagation. Hence, one can assume that this configuration corresponds to the maximum crack size allowed for the simulated loads and locations. However, results should be considered carefully. The crack assumed in this way would propagate both at interface and inside the copper material. Thus, the predefined crack propagation path, which is valid for delamination fractures, would not remain strictly true for cohesive paths, and some kinking might occur.

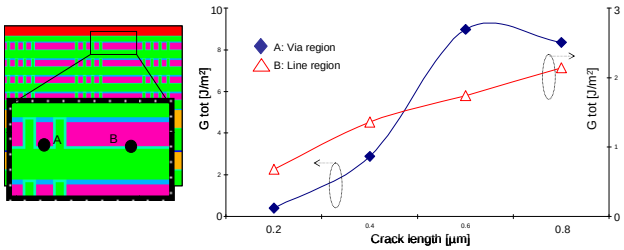


Figure 14 Energy Release Rate as a function of the crack length.

Nevertheless, aiming to increase interconnect architecture strength, this kind of behavior would deserve a deeper investigation.

5.3.4.5 Conclusions

A three-level multi-scale modeling technique is used aiming at investigating the stress state and failure hazard at the interconnect levels induced by the whole process flow of a flip-chip packaged die. This methodology enables to deal with the detrimental aspect ratios between the scales considered, and to bridge interactions between the low-k layers and the package. Furthermore, as the consecutive material deposition steps are simulated, a reliable estimation of the stress field at low-k layer is obtained.

First of all, the solution at package level is analyzed. A complex warpage pattern of the FCBGA package after Cu lid attach process is found due to the thermal mismatches between the several parts of the package.

Secondly, the interconnect pad region is particularly investigated at some locations close to the outmost bump. Both stress/strain based failure criteria and energy based failure criteria are applied at some interfaces between metal barrier and low-k dielectric. In order to point out the local interconnect layout effect, two sites, one near a via region, the other far from via, are closely analyzed.

Summary of the work is as follows:

- During interconnect build up, a cumulative phenomena is found on stress components. This leads to a global decrease of the interfacial stress field when going from the die bottom to the top.
- Effect of package stress is more complex and depends on the considered local site. When normal and shear stresses tend to increase, the contribution on the planar stress, and by consequence on the principal stress, is reversed on via regions compared to line areas.
- Energy released rate computation shows that the critical defect size is around 0.4µm, which is quite large for such structures. It means that the low-k layers of the considered device should not fail during fabrication process. This modeling result has been confirmed by reliability experiments on real CMOS90 products. Indeed, no delamination occurrence has been observed neither in line nor after aging tests.
- Aiming to go further in the investigations, energy based analysis also confirms the dependency of the results according to local layout. Most critical sites for propagation are found to be the via regions at the middle of the low-k stack. However, this statement should be considered with respect to the fact that, in such a region, a nucleated crack could be confined by metal patterns.
- Latter point is supported by the evolution of the released energy as a function of the crack size. Thus, an inflection point in the G values is found at a certain crack length which could mean that delamination phenomena would remain limited until a crack size of about 0.6µm.

Acknowledgments

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5.3.5 Chip-Package Interactions: Some Investigations On Copper/Low-k Interconnect Delaminations.

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5.3.5.1 Abstract

The introduction of brittle dielectric materials, and the feature size decrease of IC chips to follow Moore's law, are well known to pose great integration challenges. In this paper, a 3D fully parameterized Finite Elements of a Ball Grid Array package model is built and thermo-mechanical stress produced during package operations is evaluated. That aims to address FE-BE compatibility concerns. Thanks to multi level and energy based post processing methods, both analysis at the package and interconnect levels are carried out. Localized evaluation of the crack propagation likelihood into the low-k stack is performed, and several results are provided: Localisation of the delaminated interface and the particular effects of the glue fillet geometry are specially studied. Discussion on failure criteria is also proposed in order to bring inputs on dielectric damaging phenomena in advanced semiconductor products. The sensitivity to shear modes, contrary to compressive one is highlighted. On the other hand, a drastic rise of the fracture risk is suspected with highest values of the glue fillet, which might lead to delamination of the bottommost IMD layers. Possible applications of this work are the early phases of technology developments and product crisis solving.

5.3.5.2 Introduction

Aiming to improve product performances and size reductions, die interconnect features are commonly driven by electrical specifications. Among others, that leads to critical dimension decreases and new material integrations [1]. Hence, the so called Cu/Low-k couple in interconnects is nowarday widely used to reach RC specifications. However, to lower the k value the introduction of nanometric pores in dielectric materials causes weaker mechanical strenght of the die stack [2]. Hence, beyond the FEoL integration issues of low-k and ultra low-k insulators, die interconnect failures are now commonly observed during packaging tests and qualifications [3, 4]. More precisely, interfacial delamination and cracking in BEoL during packaging occur. By consequence, front and back end processes can not be separated anymore and close interactions of die and package features must be accounted as a great integration challenge [5].

Modeling is one of the major tools to understand and reduce mechanical related defects, to save trials and actual silicon, and to allow early stage development and crisis solving. However, such simulation remains a challenge and both the geometrical and failure caracteristics involved require specific methodologies [67].

In this paper, starting from experimental observations, simulation works to understand failure mechanisms and the specific effects of the die attach on chip-package interactions are carried out. A kind of loop back from experimental to modeling inputs is used to assess on numerical strategy and criteria, and then applied to increase yield of an actual CMOS90 product.

Typical observed failures

As introduced, packaged products have been submitted to thermo cycles in order to achieve a complete process qualification. These reliability tests performed during the early qualification stages with unoptimized package parameters revealed abnormally high failure rates. Analysis of the accoustic and electrical responses on failed parts determined that the location of the delamination is situated at the die corner. Then, FIB cross sections have been carried out on the die to locate more precisely the involved interface. In most of the cases, the lower part of the Inter Metallic Layers was the location of the main path for crack propagation. Figure 41 depicts a typical delamination occurrence, showing obviously that fracture propagates trought first metal and dielectric layers.

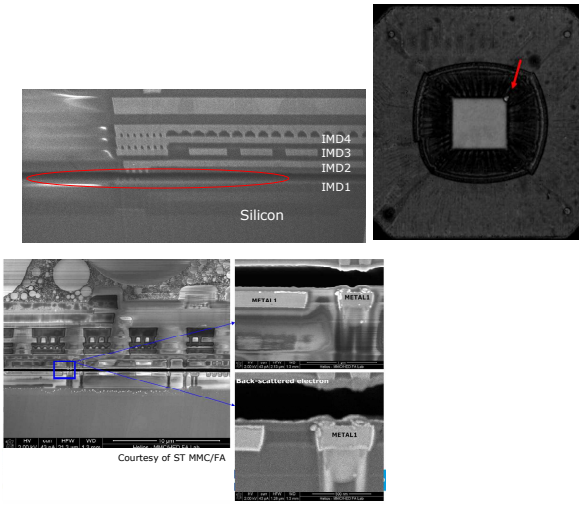

Figure 64: Cross section view of typical delamination observed in interconnects after packaged thermo-cycle tests.

In a second phase, process and parameters optimization enabled to fit with reliability spectifications; and; among others, yield values were significantly increased by a better management of the die attach features.

In the next sections, modeling strategy will be depicted, results will be discussed and faced to the below mentionned experimental inputs.

5.3.5.3 Modeling methodology

Multi scale modeling

As previously introduced, the dimension ratio from package to interconnects is about 1/500,000. It is impossible to use a single finite element model to simulate the detail of the interconnection features without a super-computer. Fortunately, sub-modeling techniques can be used to deal with this kind of problem with less computation effort.

The concept of sub-modeling is to build several models. The first one is a global model with relatively coarse mesh pertaining to the global boundary conditions (BC). The second one is called a sub-model, containing a detailed mesh for the specific area of interest. The sub-model's BC is inherited from the global model by interpolating the nodal displacements and body forces from the global model. The accuracy of the sub-model is dependent on the coarseness of the global model and the details of the sub-model. For the current problem, despite an high amount of finite elements, reliable accuracy has been obtained by the use of only two fine meshed models: A package and interconnect ones. The package model is used to assess to stress applied to the die part, and the last sub-models relates to silicon features, describing copper/low-k layout. In the first model, reliable description of the true behaviour of the die is achievied thanks to homogenisation technique, allowing to consider local design. Figure 42 shows the multi level methodolgy and homogenization flow chart.

This later thing is one of the key points of the multi-level modeling technique, i.e. the evaluation of the equivalent properties of the materials. Among the required steps, the choice of the representative unit cell (RUC) used for the homogenization is of the utmost importance. Indeed, depending on the RUC, an inaccurate evaluation of global level displacements may occur, leading to errors in the local level calculated stress and strain fields. The complete homogenization procedure used for the interconnect layers was previously studied and reported [8]. More precisely, it was shown that a simple volume averaging is unable to render the anisotropic behavior of the interconnects and that a independent discretization of the Inter Metal Dielectric (IMD) layers is mandatory.

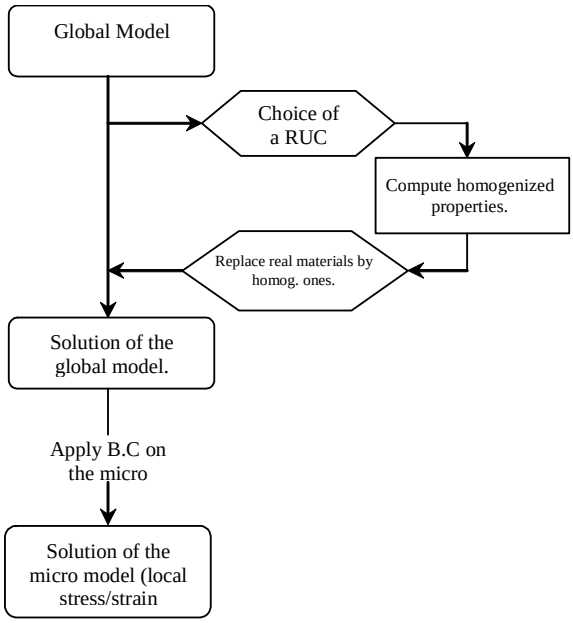

Figure 65: Multi Level and homogenization technique: Flow chart.

Fracture Mechanics

Once the strategy for the finite element models has been defined, suitable criteria must be chosen according to the observed failure modes and by taking into consideration the behavior of the material set used. Despite the fact that in-situ observations of the failure modes are tricky, the most likely scenario in our case is brittle fractures. Furthermore, micro-cracks are highly suspected to nucleate at the early stage of packaging steps such as sawing processes, which initiates local defects at the many interfaces of metal layer and low-k dielectric. Hence, the targeted failure mode, which is brittle delamination, is related to fracture mechanics and specific energy based numeric tools are developed [9, 10]. The so-called Nodal Released Energy (NRE) post processing procedure is based on the computation of energetic quantity from the nodal solution. To evaluate the NRE value, two simulations are required: One with an undamaged model, the other with the damaged one where a virtual crack has been inserted.

At this step the crack features need to be defined, particularly in terms of size and shape.

This method, easily implementable in commercial Finite Element software, enables to provides energy based quantities of the distinct opening crack modes even in complexe 3D models. Figure 43 shows the post processing flow chart and formula.

Note that the numerical parameters to be used, the sensitivity and the ability to link this value with the energy release rate has been previously validated; and additional insights compared to a standard stress based analysis have been previously demonstrated [21].

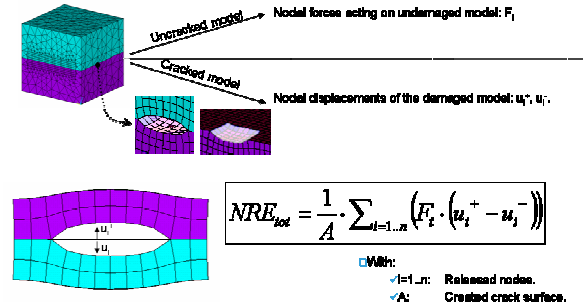

Figure 66: Nodal Release Energy (NRE) flow chart and formulae.

Models

Finite elements models

Global and local finite elements models are now built. Note that, to allow further industrial design optimizations, models are parametrized and three dimensional.

Table 7: Main model features.

		Dimension Package [mm] Interconnects [µm]	Young's modulus @[°]:[GPa]	Poisson's ratio	Coefficient of Thermal Expansion @[°]:[ppm/°]
Package	Core	13 x 13 x 0.22	19	0.3	In plane: 16.9 Out of plane: 30
	Die	6.5 x 6.5 x 0.17	130	0.28	3
	Die attach	0.02	100	0.3	0.13
	Molding compound	0.67	24	0.4	8
Interconnect	SiO2	2 thick levels + PMD	48	0.3	2.67
	Low-k	5 thin levels	8	0.15	15
	Copper		128	0.33	16.6
	Nitride		164	0.24	2.67

The main features of the models are as follows: For the global one, package type is BGA, using parts described in Table 3. The local interconnect model depicts the typical stack of an advanced CMOS90 product. The simulated die stack is seven copper metal levels (7ML) including five low-k levels and the two others containing classical silicon dioxide as dielectric. Figure 44 depicts the two models used in the multi scale simulation, a meshed interconnect pattern is provided as an example. In addtion, preliminary analysis shown that the starting location of the failure is situated at the die corner, where specific design rules are applied. Hence, models in both modeling levels account for the particular interconnect structure in that region thanks to homogenization technique and detailled meshing.

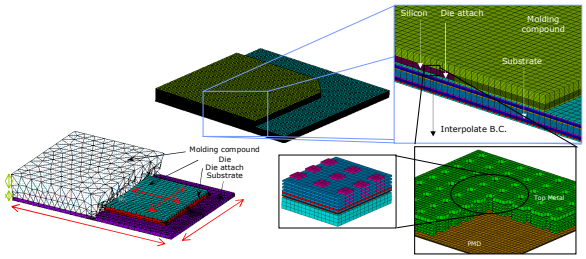

Figure 67: Package and interconnect Finite Element models.

Loading conditions

An uniform thermal variation from +150 to -40°C reproduces thermo cycling which causes the delaminations. Coeficient of thermal expansion (CTE) mismatch of materials induces device warpage and generates stress into interconnect. Actually, the likely physic governing crack propagation is here fatigue related. However, since modeling strategy is driven by the targeted application compromise must be made with industrial requirements. In this work, oriented on process and complexe structure optimization and root cause seeking, a linear fracture mechanics approach is prefered. The main drawback of this approach remains the unability to provide lifetime prediction and quantitative variations of failure rates. By consequence, uniform thermal variation corresponding to the cooling amplitude is applied, and materials are considered as stress free at initial temperature.

5.3.5.4 Simulation results

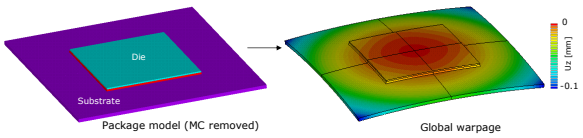

Figure 68: Global level: Package deformed shape and vertical displacement field.

Package level analysis

At first, package stress and deformation are analyzed at the global level. The distinct CTE mismatches of materials induce structure warpage. Note that deformed shape can be differents depending on package parameters ; In our application case, figure is crying with a maximum vertical downward displacement of about 100µm at the device corner. Figure 68 depicts global deformation, which has been found to be in good agreement with experimental measurements, allowing to assess on the stress free tempearature of the device.

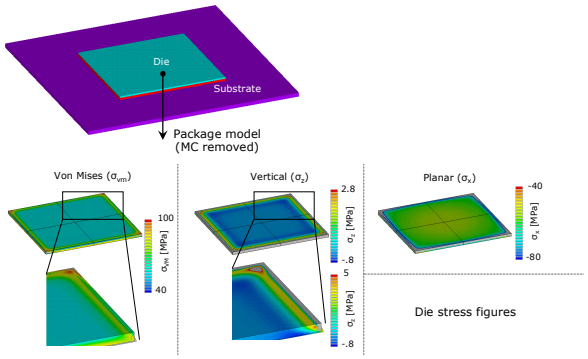

Figure 69: Die stress at global level.

Throught package deformations, die stress is generated. Figure 47 shows silicon figures and results underline a quite constant compressive deformation field in the main central region of the die. More precisely, a high planar compressive stress is found, whereas vertical component remains limited. On the other hand, stress gradients are specially observed at the die corner, where Von Mises stress becomes significant, revealing presence of shear stress components.

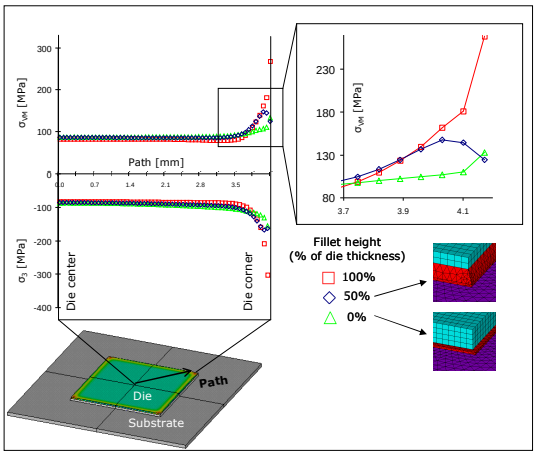

Figure 70: Package level analysis: Von Mises and compressive stress components at top die according to fillet geometry.

A deeper analysis highlights that die corner stress features are particularly affected by the die attach geometry. In order to precise these effects, several die attach geometries are simulated and stress plots are depicted in Figure 48. Results confirm that the edge regions of the die are mainly impacted, whereas the central stress field is left quite unchanged. Three die attach configurations are compared: The glue fillet height ratio between bottom and top silicon ranges from a null to a full value, and a medium case depicts a glue fillet edge coming up to the half of the silicon. Plots show that, depending on the height, both corner peak stress value and stress distribution at the die edges and corners are strongly modified. In addition, it is particularly interesting to observe that a secondary maximum stress value is located in the inner part of the die, and not only limited to the edge and corner singularities. Note that this feature could have a link with the delamination failures. Indeed, considering that the extreme edge of the silicon is compound by the sawing street, micro cracks confined in that region should not affect the reliability, at least at the first order. However, stress in the active part of the die could be more critical for reliability. Thus, by generating an higher stress at a

distance of about 200µm from the corner and hence just in the seal ring structure, the glue fillet geometry is suspected to play an important role in crack propagation during packaging tests.

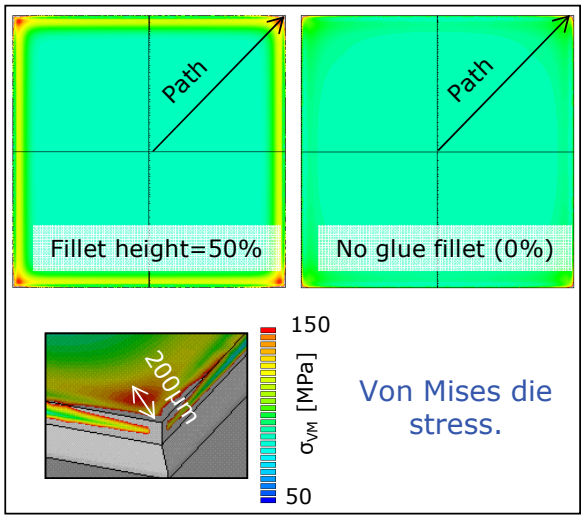

Figure 71: Package level analysis, top view of Von Mises stress at top die for the two extreme configurations of glue height.

Figure 49 compares the plane view of the stress field with the two extrem configurations of the glue fillet, revealing that peak stress is shifted inside the die. In addition, the stress principal vectors generated close to the glue edge is depicted in Figure 50.

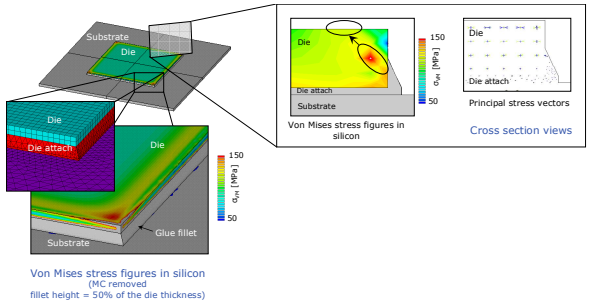

Figure 72: Package level analysis, in plane and cross section view of stress features at die corner.

Energy based analysis at low-k level and discussion

Once package stress and specific effect of the die attach have been analyzed at the global scale, deeper investigations are then carried out in the interconnect model and using the previously described energy based index. The multi scale parameters are determined thanks to the package analysis. In particular, the location of the local model is defined in the seal ring region in where peak stress and failures are observed.

This chapter aims first to discuss the suitable failure criteria to be applied and the likely location of the crack propagation within the interconnect stack. Then, insights on the risk mitigation according to the fillet height are provided, and finally learnings and discussions are proposed.

Figure 51 shows outputs from the Nodal Release Energy postprocessing method. Each value is computed are the four interfaces of the thin Inter Metal Dielectric stack as a function of the coverage ratio of the glue vs. die side. Top graph (a) shows the normal component of the released energy, this value evaluates the mode I of the crack opening. Note that, since the die is in a compressive state, the damage induced by the first opening mode is rather related to a kind of material crushing. In the next graph (b), the two other opening mode components have been summed. These ones relate to the shear propagation modes. Finally, the ratio between the two previous components is explicited is the bottom plot (c), which depicts a quantity that can be considered as the phase angle of the crack singularity. Thus, discussions are hereafter proposed from these plots and accounting on experimental insights:

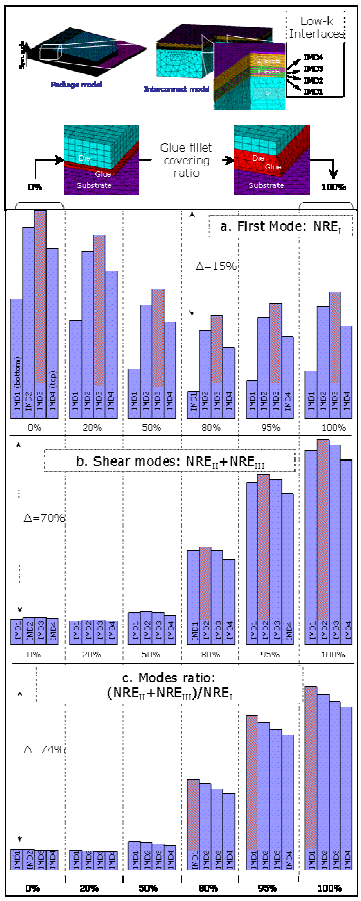

Figure 73: Interconnect local analysis: Nodal Release Energy values in several low-k layers and according to glue fillet covering ratio. (a)- First opening mode. (b)- Shear opening modes (c)- Modes ratio.

First of all, the glue fillet height value is confirmed to have significant impact on the calculated energy based values. Indeed, high variations are observed in all plots, ranging from about 15% to 70%. Nevertheless, the analysis is not so trivial since trends could be different regarding which NRE component is looked at. More precisely, the component corresponding to the first opening mode suggests that delamination should be maximized without any glue fillet. At the contrary, shear modes and mode mixity show highest values with a full covering ratio.

However observations underlined that, on one hand delaminations are typically observed in the bottom low-k layers; furthermore significant yield change was obtained with a better control of the glue fillet. On the other hand, modeling results shown in the top plot do not fit with the later facts, whereas the two other figures agree these two points. Hence, experimental insights assess on the most relevant criteria to apply, and suggest to engage discussions.

As a first consequence on the damaging mode of the used low-k material, compressive stress state would not lead to weaken low-k interface. This was indeed initially quite unknown, since the intrinsic porous feature of the material structure, could have made it sensitive to crushing phenomena. Hence, fracture occurrence would be here rather related to crack propagation thank to shear opening modes, which was not a priori easy to guess. As a general remark, it must be noticed that in any simulation, notably because critical adhesion values are strongly dependent on the mode mixity, the most relevant criteria to account is a key concern.

Thus, as depicted in bottom plots of Figure 51, shear modes and mode mixity values reveal that the effect of the glue height remains limited in the cases of low covering ratio. But for highest glue fillet, i.e. from about 50%, NRE values increase drastically and the maximum is reached with a fillet covering the whole silicon edges.

5.3.5.5 Conclusions

Motivated by yield loss during qualification tests and based on experimental investigations, thermo-mechanical simulations have been carried out to address some chip-package interaction concerns. In this paper, the dedicated modeling methodology, including multi level and three dimensional energy based post processing is presented and applied on an actual 90nm product. The preliminary analysis at the package level underlines the particular effect of the glue fillet height on the corner die stress features. Then, thanks to in house energy based criteria, localized evaluation of the crack propagation likelihood into the low-k stack is performed. Several kind of results are provided, localisation of the delaminated interface and the particular effects of the glue fillet geometry are specially studied. Discussion on failure criteria is also proposed in order to bring inputs on dielectric damaging phenomena in advanced semiconductor products. The sensitivity to shear modes, contrary to compressive one is highlighted, and released energy plots indicate an higher delamination hazard in the bottommost IMD layers. On the other hand a drastic rise of the fracture risk is suspected with highest values of the glue fillet.

Acknowledgments

Thanks are due to colleagues from Grenoble and Crolles ST manufacturing sites, package experts from Toa Payoh modeling team, particularly Pascal Scafidi, Jaspreet Sidhu, Anne Laffont and Jing En Luan for their fruitfull inputs.

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5.3.6 Method for managing the stress due to the strained nitride capping layer in MOS transistors

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5.3.6.1 Abstract

Since the 90nm CMOS technology node, the strained nitride capping layer (CESL) is used as a stress-engineering booster enabling transistors improvement. This paper presents a complete mechanical simulation work explaining how the Contact Etch Stop Layer (CESL) transmits its intrinsic stress to the Si-channel. First, it is demonstrated that the CESL stress transmission is the outcome of several CESL parts acting separately (direct effect) or in association (indirect effect) without neglecting the corner effects for small transistors. Then, all the different contributions of these CESL parts on the stress transfer way for long and short channels are explained. Finally, some guidelines are given for an optimization of the CESL use.

5.3.6.2 Index Terms

Contact Etch Stop Layer (CESL), stress, explanation on the transmission way of the CESL intrinsic stress, optimization, Si-channel state of stress

5.3.6.3 Introduction

Transistor scaling down has been the primary factor driving CMOS performance improvement for more than 30 years. Approaching the fundamental limits of transistor scaling leads the industry and the research community to actively search for alternative solutions [1,2]. In this context, the use of strained-Si layers obtained by stress-engineering seems to be one solution to achieve transistor performance improvements [3,6]. In fact, one knows that the electrons mobility in the NMOS devices (respectively the holes mobility for PMOS) can be changed depending on the state of stress in the channel [7]. Moreover, stress-engineering is a low cost way to boost the CMOS technology.

The Contact Etch Stop Layer (CESL) for inducing strain is one of the possible solutions amongst all the feasible stress-engineering boosters (strained-spacer, silicide, SiGe, strained-gate…). The CESL consists in a nitride layer used to stop the etching of the metallic contact. By modifying the deposition recipe, the intrinsic strain of CESL can be compressive or tensile. The usual thickness of CESL varies from 20nm up to 100nm according to the deposit time, and its thickness uniformity depends strongly on the deposit process tool (uniformity about 70% for PECVD, about 90% for ALD).

Many studies have highlighted that the impact of CESL on the channel state of stress depends on various parameters, like gate length and height, spacer shape, presence of contact holes, CESL thickness and stress [8-12]… But so far, the effects of CESL are only observed thanks to electrical measurement data explained by simple mechanical simulations. In this paper, a complete mechanical simulation work has been performed in order to explain in details how the CESL transmits stress to the Si-channel. Thus, the CESL stress transmission way is complex; it is the outcome of several CESL parts acting separately (direct effect) or in association (indirect effect) without neglecting the corner effects. Thus, based on the study of the channel state of stress induced by the CESL for long and short channels, the aim of this paper is to list, explain and quantify all the different contributions of these CESL parts on the stress transfer way. Then, based on this understanding, the impact of all the previous named parameters will be easily explained. Finally, guidelines for CESL optimization are given.

5.3.6.4 Modeling strategy

In order to investigate the CESL stress transmission, finite element simulations were performed using Ansys software.

A. Model description

The CESL effect has been investigated on transistors isolated each others by STI thanks to a 3D model parameterized according to gate dimensions and CESL characteristics. Thanks to symmetries, only a quarter of the full 3D transistor has been simulated as illustrated in figure1. The X direction is the gate length direction, Y

direction corresponds to the width of the channel and Z direction represents the vertical direction. In this study, the CESL layer thickness is 60 nm, gate length varies from 32nm to 1µm and the gate width is equal to 1µm. The choice of dimensions has been motivated by electrical results showing CESL impact which enables to validate the mechanical simulations. Nevertheless, the conclusions are still valid for other devices dimensions and can be easily extended to other CESL characteristics.

As illustrated on figure 2, the CESL layer has been split in three distinct zones making up of the whole nitride capping layer:

- top-CESL above the gate region
- lateral-CESL above the spacer region
- bottom-CESL above source/drain and STI region

Thus, the thickness and the intrinsic stress of each zone can be different from others. The classical CESL is the sum of these 3 CESL zones having the same thickness and the same intrinsic stress. The aim of this virtual splitting is to determinate the contribution of each CESL zones on the channel state of stress along X, Y and Z directions.

B. Assumptions

In this study, the CESL intrinsic stress is tensile and equal to 1GPa. It is assumed to be a biaxial stress following the curvature of the deposited layer. This biaxial stress has been implemented in the model as an intrinsic stress oriented along a local work plane, which its orientation follows the CESL curvature thanks to a meshing element re-orientation as schematically explained in figure 1. In order to clearly analyse the relative contribution of the strained CESL only, all the materials are stress free except the nitride capping layer. Thus, the stress state of Si-channel is here only due to the CESL intrinsic stress. An elastic behaviour is assumed for all materials. So in these conditions, the contribution of others stress sources like STI could simply be added to the CESL one.

C. Accuracy validation

Prior to explaining the CESL stress transmission way, it is mandatory to verify the accuracy of the model. First, a qualitatively comparison on stress distribution in the device, obtained by FE modeling and by physical characterization techniques like CBED and µRaman, has been made. Subsequently, a quantitative validation based on electrical results has been obtained thanks to the development of a complete TCAD methodology combining mechanical and electrical simulations. Briefly, the electrical simulations rely on a set of strain dependent mobility models derived from strained full-band Monte Carlo simulations. This allows handling non-constant stress fields as obtained from mechanical simulations. Doping profiles have been carefully calibrated upon control stress "free" experimental data.

In figure 3, the simulated on-state current enhancement percentages (A) for a given off-state leakage as a function of the gate length are compared to silicon measurements for two CESL conditions. Note also that two averaging procedures have been used and compared in order to stick to convenient 2D strain fields. The first approach (pseudo-3D) consists in assuming that the 3D MOSFET's can be regarded as the sum of elementary 2D slices mounted in parallel for which the strain field is averaged along the y direction over each section. In the second approach, the strain field is implemented in a single 2D transistor and is only described by two constant strain regions obtained by averaging the strain components over the volume of respectively the source-drain extensions and the channel. The figure 3 highlights that the experimental curves are well reproduced by the pseudo-3D approach: the discrepancies are within the uncertainties on the intrinsic stress level and thickness of the CESL on a patterned wafer and on process simulations. The simplified constant strain fields approach also captures most of the experimental features but the accuracy is somewhat lower. Thus this simulation chain can be regarded as a sound basis to analyze these experimental data and give insight on the scalability of the performance enhancement.

Note that, the stress, represented on following graphs, corresponds to the average stress in the Si-channel (depth = 1nm, width = gate width).

5.3.6.5 Results

A. Long Transistors

Typical stress fields generated by a tensile CESL are depicted in figure 4 for long transistors. CESL induces mainly a compressive stress whatever the stress components. Nevertheless, the state of stress along Z direction is quite uniform and compressive, whereas along X and Y directions, there are two distinct areas; a compressive one near the channel centre and a tensile one near the channel edges. The compressive area takes up about two thirds of the channel and the tensile area about one third.

B. Small Transistors

Contrarily to long transistors, CESL induces a tensile stress along X and Y directions whereas stress in Z direction remains compressive (Figure 5). Here, the state of stress is uniform whatever the considered direction.

C. Impact of CESL Intrinsic Stress Level

According to our assumptions, results with other CESL intrinsic stress levels could be deduced thanks to a proportional rule. Therefore, the next analyses are still valid. For a compressive CESL, the tensile area in the channel will become compressive and the compressive area will become tensile.

5.3.6.6 Analysis

A. Analysis of CESL Effects on Horizontal Stress Components

The direct effects of each CESL zones are responsible of the Si-channel stress state. The direct effect of one CESL zone is defined as the impact of this CESL zone on one's own without the two others CESL zones. Figure 6 schematizes the three direct effects corresponding to the three CESL zones. To estimate clearly the direct effect of a single zone, two over the three CESL zones have been removed successively in the model as explained in figure 7. Figure 8 represents the impact of a single CESL zone on the resulting average stress in X, Y or Z direction. On the same figure, the impact of a standard uniform CESL covering the whole transistor is also indicated as a reference value. It can be noted that the influence of each of these three zones has a specific impact which depends strongly on the gate length. The top-CESL leads to compressive stresses in the channel for large gates and its impact decreases with the reduction of the gate width. Thus, no effect is found for narrow gate (L=65nm). The lateral-CESL leads to compressive stresses in the channel also but its impact increases drastically when the gate width decreases. The bottom-CESL adds tensile stresses in the channel and its impact increases also drastically when the gate width decreases. By comparing the stress state induced by each of these three CESL zone to the classical CESL, we can conclude that:

- the classical CESL stress in X direction is mainly due to the direct effect of the bottom-CESL,
- the classical CESL stress in Y direction is small due to the contrary effect of each direct effect,
- the classical CESL stress in Z direction can not be explained by any of the 3 direct effects.

Figure 9 explains how the bottom-CESL transmits its stress to the channel. Considering a tensile CESL, the mechanical equilibrium is reached by decreasing the bottom-CESL zone size in X and Y directions. As this bottom-CESL is attached to the spacer and to the silicon, this size decreasing is limited because it leads to tensile stresses in X and Y directions.

B. Analysis of CESL Effects on Vertical Stress Components

The aim of this paragraph is to highlight that the stress in Z direction is due to the CESL indirect effects. The indirect effects are defined as the impact of a CESL zone in interaction with the two others CESL zones.

Figure 10 schematizes the three indirect effects corresponding to the three CESL zones. For example, the indirect effect of the bottom-CESL applies a vertical force on the Si-channel by pulling on the top-CESL via the lateral-CESL. This indirect effect could be compared to the mechanical force needed to remove a fold in the centre of a carpet (fold=gate+spacer; pull force at both carpet sides= indirect effect of bottom-CESL)! To better understand the role of these indirect effects, the deformed shape of a long transistor is plotted in figure 12. Like for the direct effect, there are 3 different indirect effects corresponding to the three CESL zones. Which one of these three indirect effects is responsible for the stress in Z direction? The methodology set up to answer to this question has been to keep the whole CESL but by taking into account intrinsic stress only in one CESL zone (the two others are stress free) as explained in figure 12.

Figure 13 represents the map of stress in Z-direction due to indirect effects for long gate (l=1µm), the map of stress obtained with the whole CESL is also indicated. Figure 13 demonstrates that the compressive stress along Z direction is only due to the indirect effect of the Top-CESL. For short gates, the indirect effects of each CESL zones contribute to the compressive stress along Z direction: Lateral-CESL has the main impact (about 49% of the total stress amount with the whole CESL, figure 14), then Top-CESL contributes of 29% and 21% for Bottom-CESL.

C. Impact of Gate Length Decreasing

The non-uniformity of stress field in X and Y directions for long transistors as the uniformity for short transistors can be explained by considering a corner effect. The corner effect is due to the interaction of the lateral-CESL and the bottom-CESL. It is responsible of the stress fields disruptions observed near the bottom edge of spacers. Figure 15 presents the stress evolution from a long device to a short one. The compressive and the tensile areas are represented on this map of stress by red and blue dotted lines respectively. Figure**Error! Reference source not found.** shows that, by decreasing the gate length, the size of the compressive area (in X and Y directions) is reduced whereas the size of the tensile area remains the same. For short device, this corner effect has major impact which explains the state of stress in X and Y directions. For long devices, the corner effect is responsible for the non-uniformity of the stress field.

D. Summing-up of the impact of all the CESL effects

Table 1 sums up the impact of all the CESL effects (C=corner, D=direct, I=indirect) for each CESL zones (Top, Lat=Lateral and Bot=Bottom). For long and short channels, corner effects induce tensile in-plane stress, bottom-CESL induces tensile in-plane stress Top and Lateral-CESL lead to compressive stress (in and out of plane) and indirect effects are responsible for the stress in Z-direction.

The major effect is the corner for short channel, whereas for long channel direct effects are dominant.

Table 1 could be very useful to estimate qualitatively the impact of parameter modification without any FE computation. Let's see for example the impact of a spacer shape modification. Two types of spacer shapes are commonly used; a D-shape or L-shape as illustrated on the figure 16. A finite element calculus points out that the stress in X-direction in the Si-channel is higher with a L-shape spacer (270MPa) than a D-shape spacer (224MPa), whereas it is the inverse for stress in Z-direction (L-shape=-176.1 MPa, D-shape: -195.6 MPa). This result can be rediscovered with the use of table 1. Indeed, table 1 indicates that the stress in X-direction is due to the "direct effect" of the bottom-CESL. With an L-shape spacer, this effect will be higher because that it is closer to Si-channel. Table 1 indicates also that stress in z-direction is due to the "indirect effect" of top-CESL, lateral-CESL and bottom-CESL. All these indirect effects have a stronger impact for an L-shape spacer because the higher the angle of spacer, the higher the force in Z-direction transmitted, as schematically explained in figure 17.

Thus, one can see that the direct and indirect effect balance of the 3 CESL zones depends on the MOS design. However, the tensile or compressive effect of one zone will be kept, so table 1 is still valid whatever the MOS design.

V. Optimization of CESL Use

The different impact of these three zones can be exploited to reach the best stress configuration that enables us to have the best performance for both NMOS and PMOS devices. In fact, the use of the classical CESL has 2 major drawbacks: In one hand, 2 different intrinsic stresses for the nitride layer must be used to optimize NMOS and PMOS at once: A compressive CESL is needed to optimize PMOS and a tensile CESL to optimize NMOS. So, the performances of NMOS and PMOS transistors cannot be enhanced using the same CESL. On the other hands, the stress map in the channel is affected by the layout. So, it is very hard to ensure the same performance to several transistors. Thus, a simple use of the CESL does not enable to fully manage the stress configuration in the Si-channel.

A. CESL with non-uniform thickness or non-uniform strain

A method for managing the stress configuration in the channel thanks to an engineered CESL is proposed. As a matter of fact, the stress in the channel can be controlled and so optimized by adjusting either the thickness or/and the intrinsic stress of the different CESL zones. Thus, the suitable combination of these three zones permits in particular to lead to the maximum electrical performance for NMOS and PMOS but also according to a wide range of layouts.

For NMOS, it has been observed that it is advantageous to have a large ratio (for example greater than 100 %), and preferably as high as possible between the top CESL-zone and the lateral CESL-zone, whereas it is advantageous to have a small ratio (for example around 50 % or smaller), and preferably as small as possible between the top CESL-zone and the bottom CESL-zone.

For PMOS, a top/lateral CESL-zone ratio is preferably as low as possible, (for example around 50 % or smaller) whereas the top/bottom CESL ratio is preferably as big as possible, (for example greater than or equal to 150 %).

Departing from these general considerations about the different ratios, the man skilled in the art will be able to define precisely the desired pattern of the engineered CESL depending on the desired mobility improvement of the transistor.

B. Method for managing the strained CESL

Many possibilities exist for obtaining an engineered CESL. One solution for having a thickness engineered CESL consists in patterning said initial CESL by etching partially and locally the initial CESL. Indeed, the top zone or the bottom zone of the CESL can be removed thanks to an anisotropic etch to obtain a 3D-patterned CESL. One solution for having an intrinsic stress engineered CESL consists in locally relaxing the stress of the initial CESL for example by germanium implantation.

5.3.6.7 Conclusions

The CESL stress transmission to the Si-channel is investigated. The results show that the Si-channel state of stress is caused by 3 distinct effects. Some effects will become more significant as channel length is further reduced. A table, summing-up all the impact of these effects, can be used to estimate qualitatively the impact of parameter modification as spacer shape or CESL morphology.

5.3.6.8 References

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TABLE CAPTIONS

Table 8: Summing up the impact of all the CESL effects (C=corner, D=direct, I=indirect) for each CESL zones (Top, Lat=Lateral and Bot=Bottom).

FIGURE CAPTIONS

Figure 74 : View of a quarter of the meshing of the whole geometry.

Figure 75: Schematic representation of the 3 zones (top-CESL, lateral-CESL, bottom-CESL) making up of the whole CESL.

Figure 76: Comparison of the simulated saturation current enhancement ratio to experimental data as a function of the gate length

Figure 77: Top view of a quarter of the channel stress fields for long devices (gate length = 1µm).

Figure 78: Top view of a quarter of the channel stress fields for short devices (gate length = 65nm).

Figure 79: Schematic representation of the direct effects of the top-CESL, lateral-CESL and bottom-CESL zones

Figure 80: Illustration of the methodology set up to investigate the impact of direct effect.

Figure 81: Impact of the 3 direct effects on the average channel stress versus the gate length.

Figure 82: Explanation on the bottom-CESL zone stress transmission way to the channel.

Figure 83: Schematic representation of the indirect effects of the top-CESL, lateral-CESL and bottom-CESL zones

Figure 84: 3D view of a transistor deformed in Z direction due to the indirect effects. (note that for clarity purpose, the deformations are scaled by 100)

Figure 85: Illustration of the methodology set up to investigate the impact of indirect effect.

Figure 86: Map of stress in Z-direction due to indirect effects compare to the stress obtained with the whole CESL for long gates (l=1µm)

Figure 87: Map of stress in Z-direction due to indirect effects compare to the stress obtained with the whole CESL for short gates (l=65nm)

Figure 88: Stress fields evolution from a long device to a short device (view of a quarter of whole the channel)

Figure 89: 2 types of spacer shape

Figure 90: Schematic impact of indirect effects vs. 2 spacer shapes

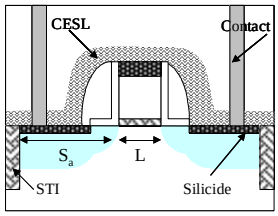
TABLES

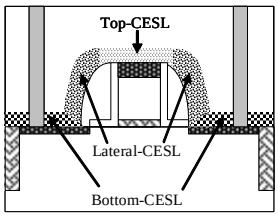
Table 1

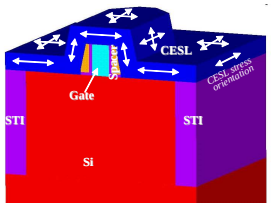
		Corner	Top	Lat.	Bot.
Long	Sx	C^+	D^-	0	D^+
	Sy	C^+	D^-	0	D^+
	Sz	0	I^-/D^-	0	0
Short	Sx	C^+	0	D^-	D^+
	Sy	C^+	0	D^-	D^+
	Sz	0	I^-	I^-/D^-	D^-

LEGEND:

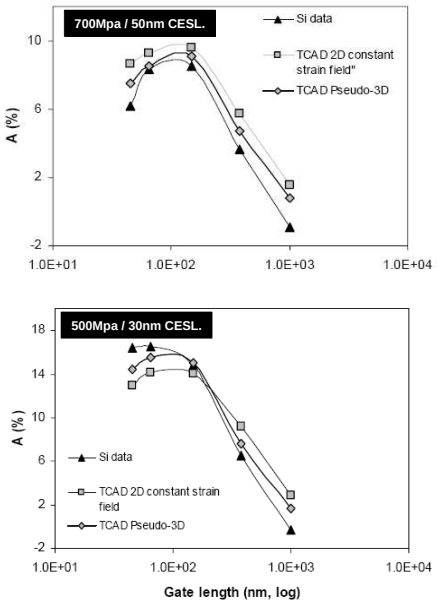
C : Corner effects
D : Direct effects
I : Indirect effects
- : Compressive stress
+ : tensile
0 : no or low impact

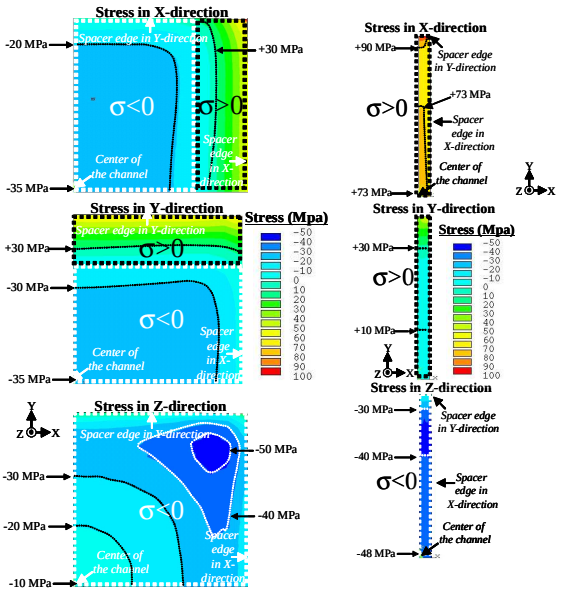


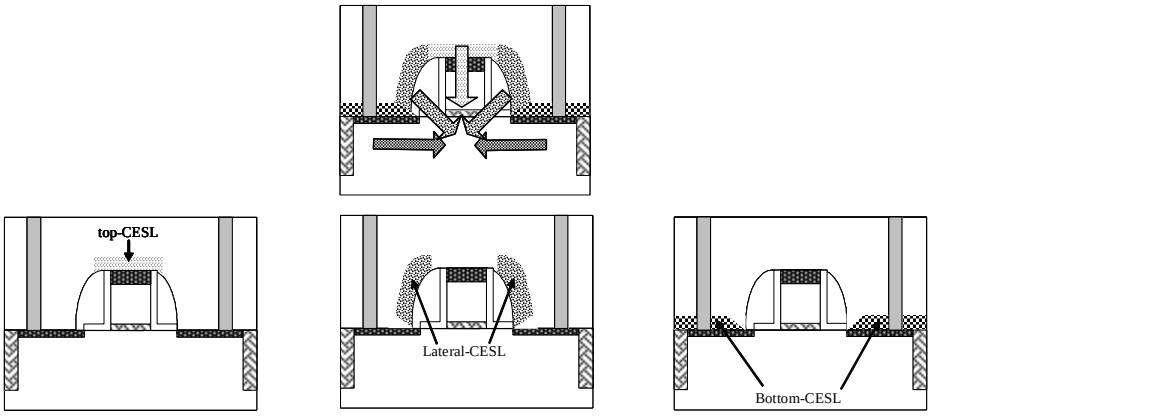


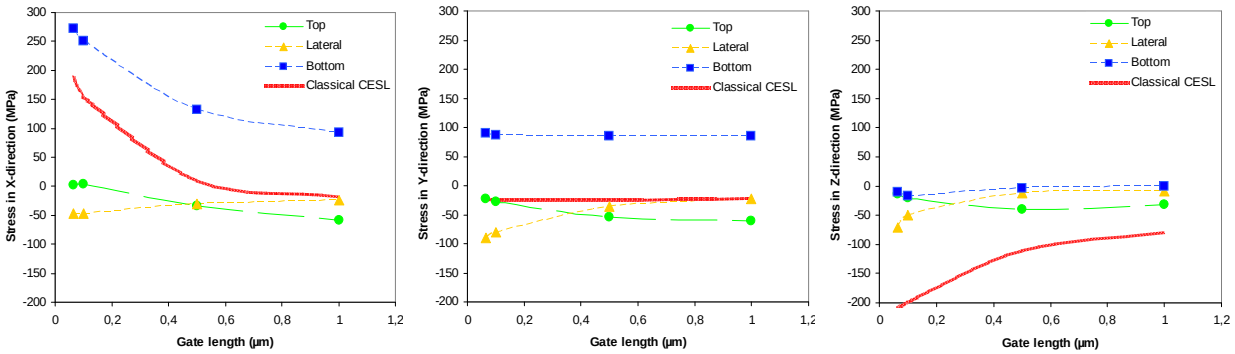


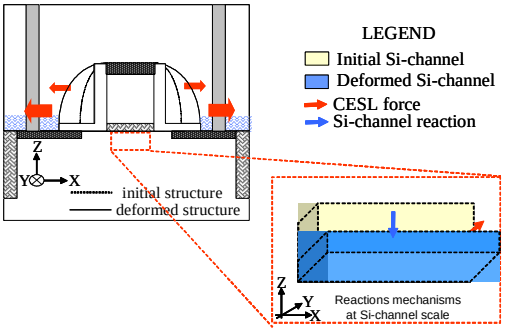
FIGURES

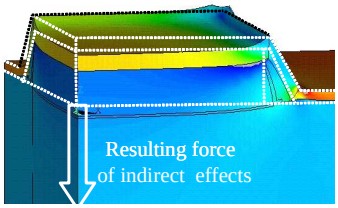

700Mpa / 50nm CESL.
Si data
TCAD 2D constant strain field"
TCAD Pseudo-3D
A (%)
500Mpa / 30nm CESL.
Si data
TCAD 2D constant strain field
TCAD Pseudo-3D
A (%)
Gate length (nm, log)

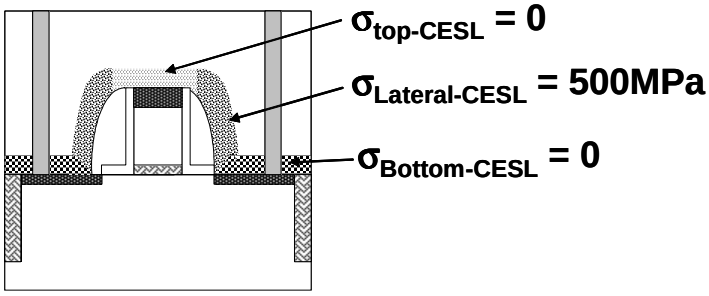

Stress in X-direction
Spacer edge in Y-direction
-20 MPa
+30 MPa
σ<0
σ>0
Center of the channel
Spacer edge in X-direction
-35 MPa
Stress in Y-direction
Stress (Mpa)
Spacer edge in Y-direction
+30 MPa
-30 MPa
σ>0
σ<0
Center of the channel
Spacer edge in X-direction
-35 MPa
Stress in Z-direction
Spacer edge in Y-direction
-50 MPa
-30 MPa
σ<0
-40 MPa
-20 MPa
Center of the channel
Spacer edge in X-direction
-10 MPa
Stress in X-direction
+90 MPa
Spacer edge in Y-direction
+73 MPa
σ>0
Spacer edge in X-direction
Center of the channel
+73 MPa
Stress in Y-direction
Stress (Mpa)
+30 MPa
σ>0
+10 MPa
Stress in Z-direction
-30 MPa
Spacer edge in Y-direction
-40 MPa
σ<0
Spacer edge in X-direction
Center of the channel
-48 MPa

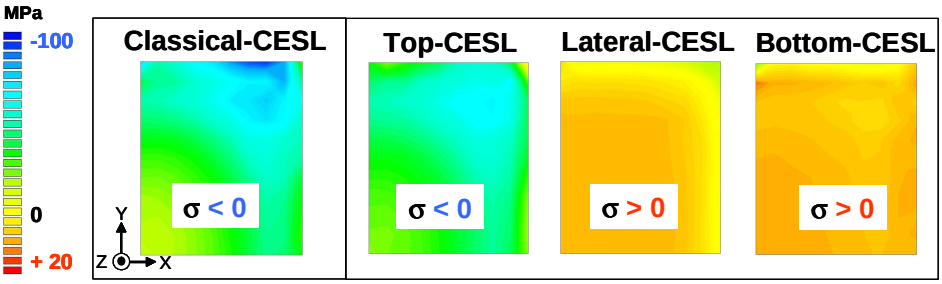

top-CESL
Lateral-CESL
Bottom-CESL

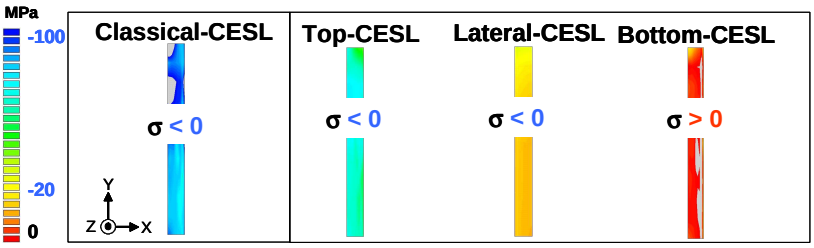

Top
Lateral
Bottom
Classical CESL
Stress in X-direction (MPa)
Stress in Y-direction (MPa)
Stress in Z-direction (MPa)
Gate length (µm)

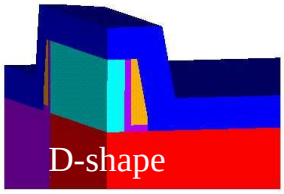

LEGEND
Initial Si-channel
Deformed Si-channel
CESL force
Si-channel reaction
initial structure
deformed structure
Reactions mechanisms
at Si-channel scale

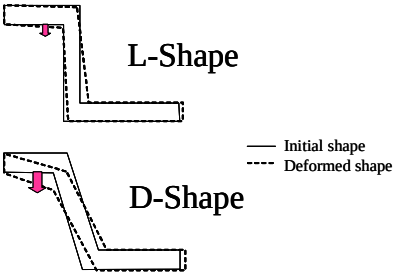

Resulting force
of indirect effects

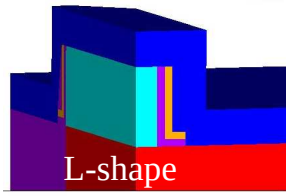

σtop-CESL = 0
σLateral-CESL = 500MPa
σBottom-CESL = 0

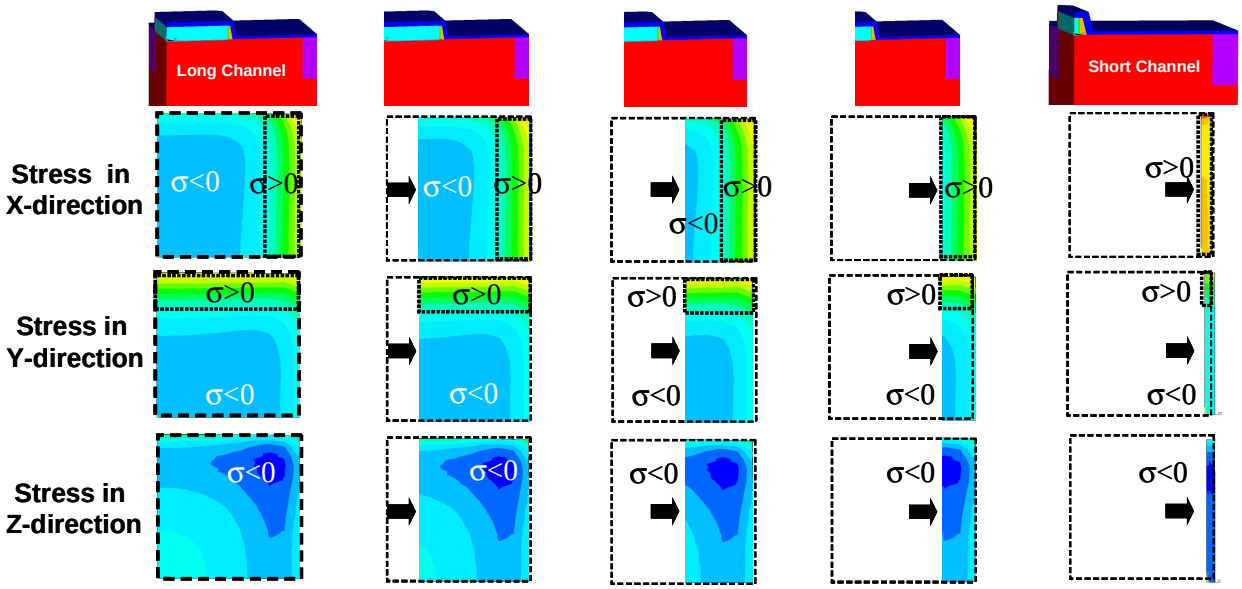

MPa
-100
0
+ 20
Classical-CESL
Top-CESL
Lateral-CESL
Bottom-CESL
σ < 0
σ < 0
σ > 0
σ > 0


MPa
-100
-20
0
Classical-CESL
Top-CESL
Lateral-CESL
Bottom-CESL
σ < 0
σ < 0
σ < 0
σ > 0


D-shape


L-Shape
Initial shape
Deformed shape
D-Shape


L-shape


Long Channel
Short Channel
Stress in X-direction
Stress in Y-direction
Stress in Z-direction
σ<0
σ>0

5.3.7 Thermo-Mechanical Modeling Of Process Induced Stress: Layout Effect On Stress Voiding Phenomena

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5.3.7.1 Abstract

Stress migration is one of the major failure causes in copper interconnects. Moreover, for a given technology and a given process flow, one can wonder if the metal layers layout could play a role in this phenomenon. The aim of this work is to numerically investigate if the presence of a high metal density value at the top layers can subsequently modify the stress migration hazard. Such a scenario has been highly suspected by experimental data. Indeed, several back end architectures have been implemented, reliability tests have been performed and compared. Measurement data shows that migration results are dependant of the interconnect layout. In this paper, the developed modeling methodology is presented: More precisely, the step by step modeling of the whole process flow enables to provide the stress field induced by the coefficient of thermal expansion mismatch of the consecutive material deposits. In this two dimensional simulation, both void nucleation and growth are analyzed. This work focuses on the mechanical stress induced by the process steps from the 4th metal level to the passivation layer deposit regarding the metal density at the above layers. Stress voiding risk in the reliability structures with and without the bond pad above is then evaluated and compared for narrow and wide lines. Results highlight some high differences in the induced stress field, and likely sites for void nucleation and growth are suggested. More precisely, two sites are found to be good candidates regarding the stress voiding phenomena: Firstly, the bond pad edge and secondary, all the transition areas between the metal lines and the dielectric at the Metal 4 level. This enables a smart management of the interconnect stress state by providing suitable design rules at the above layers.

Keywords: Stress migration, finite element simulation, mechanical modeling, stress gradient, interconnect reliability, bond over active.

5.3.7.2 Introduction

Stress voiding phenomenon is one of the major failure causes in copper interconnects. Stress migration has been widely studied for advanced semi conductor products. Among previous modeling works, most of the studies have consisted in investigating the stress migration phenomenon for an isolated pattern of interconnects. More precisely, stress field in a chain made of two copper lines connected by a via has been deeply studied and trends concerning the local stress migration phenomenon are provided [1-2-3]. However, in order to address with accuracy the stress migration phenomenon, a reliable estimation of the stress field in the area of interest is mandatory. Several aspects must be considered in order to reach this objective from a modeling point of view. Among these, both the process induced stress [4] and the environment at the vicinity of the interested locations must be taken into account. In that sense, for a given technology and a given process flow, one can wonder if the metal layers layout could play a role in this phenomenon.

This effect has been highly suspected by experimental data: Classical reliability structures, bordered by hillock detectors, have been implemented in a 6 metal levels test vehicle. The reliability structures, which are representative of the active part of die, can be underneath the bond pad structure or not. Hence, in order to validate this so-called Bond Over Active (BOA) process, reliability tests have been performed and compared for lines with and without the BOA structure above. Two line widths have been implemented with extrusion detectors around, and resistance measurements in accelerated conditions of aging have been analysed. Reliability data shows that migration results are weaker in the

case of the BOA technology. On the other hand, this trend is not affected by the probing and the bonding conditions, meaning that the layout change is the root cause of the observed differences.

The aim of this paper is to numerically determine if the presence of high metal density value at the top layers subsequently can induce changes in the stress field in the lower metal levels and by consequence modify the stress migration hazard. Step by step modeling of the whole process flow to evaluate the stress induced in copper lines is performed: This provides the exact stress field induced by the coefficient of thermal expansion mismatch and the consecutive material deposits. In this paper, the process induced stress is evaluated for two distinct structures.

First of all, the two simulated stacks will be described. Then, the modeling strategy aiming at simulating the whole process flow is explained. Considerations on the rheological behaviour of the involved material will be discussed. Finally, two dimensional simulations along different cross sections will be performed and criteria applied on the resulting stress field will be applied, thus enabling to compare the stress migration hazard in the two considered structures.

5.3.7.3 Modeling strategy

5.3.7.3.1 Finite Element Model

FIGURE 91 shows schematic top views of the BOA and standard simulated reliability structures. More precisely, at the metal 4 level, two widths for the electro migration lines are tested: 0.2µm and 3µm. Each line is bordered by hillock detectors used to ensure a suitable detection in case a migration phenomenon occurs in the tested line. The change in the structures concerns the upper Inter Metal Dielectric (IMD) levels. In the case of the BOA structure only, a bond pad is built up with copper lines at the metal 5 and metal 6 levels. At the metal 5 level, a periodic sequence is designed. A plate of copper in the whole area of the pad compounds the metal 6 layer.

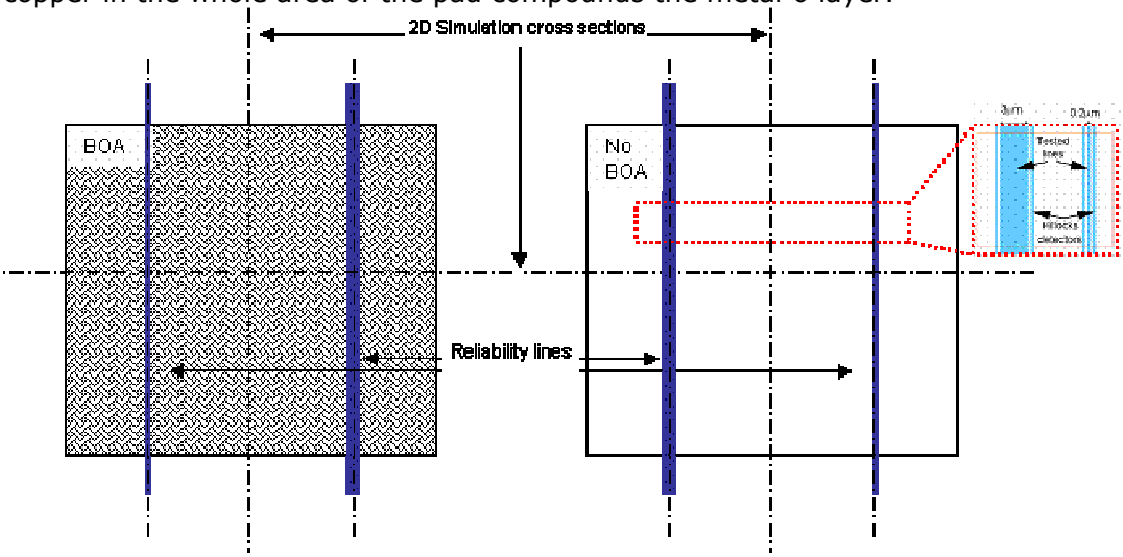
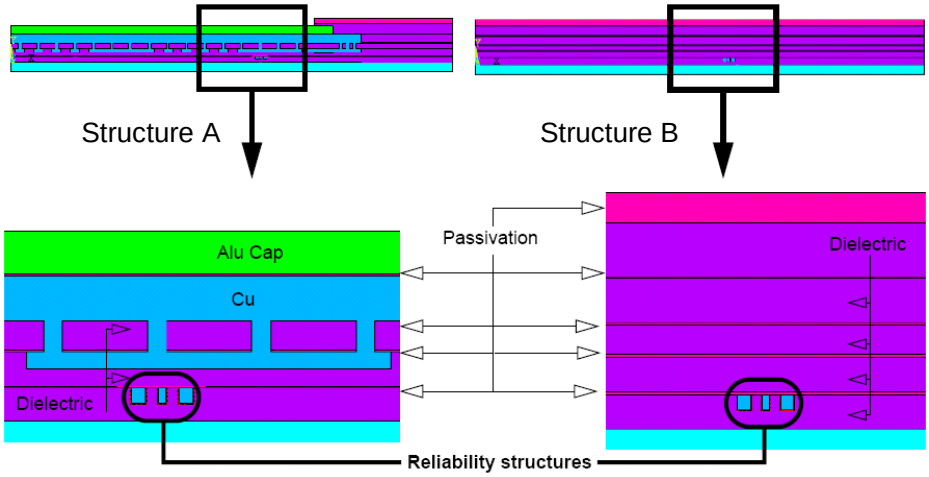


FIGURE 91. Schematic plane view of the simulated structures (left: with BOA structure, right: without BOA). Right scheme shows zoomed view of the reliability lines.

Several modeling aspects may be noticed: The ratio between total dimension of the bond pad and the copper line width leads to a high amount of finite elements in order to describe the structure. In addition, a lot of solving operations are needed to reproduce the process flow. Taking into account these modeling considerations, only two dimensional analyses can be performed in a reasonable CPU time and choice must be made concerning the simulated plane. More precisely, with respect to the tested line direction, two perpendicular cross sections (lengthwise and widthwise) are considered in this study.

Some of the other characteristics and assumptions of the model are listed below: (i)Since a high number of bond pads are aligned, symmetrical boundary conditions are applied to the edge of the structure and only a half of the bond pad is simulated. (ii)The process steps from the third Inter Metallic Deposit (IMD3) to the passivation layers are simulated in order to render the deposit temperature of each layer. (iii)In order to reach more accurately the stress field in the reliability structures, the TaN barrier layer is modelled at the metal 4 level. However, the contribution of this thin

layer is neglected in the pad levels. (iv)All layers are assumed to be planar, in particular the bond pad



passivation layer. A comparative scheme of the structures is depicted in **FIGURE 92**.

FIGURE 92. Example of the simulated structures: Left: Structure A with metal lines at the 4th ML and some patterned metal lines at the top layers. Right: Structure B with only the tested lines at the 4th metal level (ML) and no metal at the above layers.

5.3.7.3.2 Material Properties

In order to evaluate the stress field with the topmost accuracy, it is necessary to pay a particular attention on the rheological model to be used. Nevertheless, in the considered case, a simple liner elastic assumption seems to be the most suitable: in terms of temperature dependence, the material properties are assumed to be constant in the considered temperature range. For non metallic materials and at low temperature, the oxide layers, TaN and SiN, show an elastic behaviour [5]. However, the mechanical behaviour of copper is more confused: The microstructure, and consequently the mechanical properties, is connected to the width of the copper line. Moreover, performing measurements on patterned wafers is arduous and results are, at the present time, quite partial. On the other hand, the microstructure of the copper may change during the process steps showing a non-linear behaviour. At last, the copper layer is deposited by two different processes: a thin layer is firstly deposited by PVD, and then the other part of the layer comes from ECD growth. It is likely that these two layers have distinct mechanical behaviours. Finally, in this simulation, the copper material is modelled as an elastic isotropic material, with a stress free temperature set at 200°C, and the full copper thickness is considered to be homogeneous.

Thus, taking these assumptions and the state of the art concerning the rheological model of the copper into account, the envisaged comparative analysis can be performed.

Material properties are summarized in Table 9: E corresponds to the Young's modulus, ν to the Poisson's ratio, CTE to the Coefficient of Thermal Expansion and the last column depicts the temperature at which the material is free of stress.

TABLE 9. Mechanical properties of materials

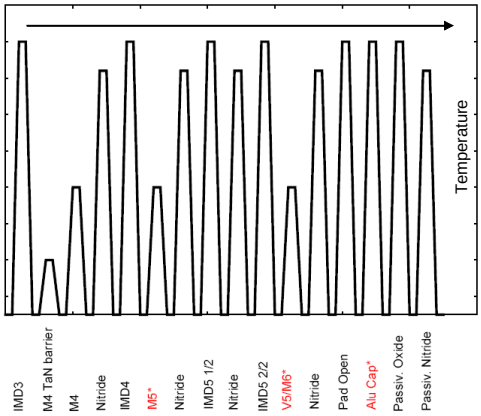
	E [GPa]	ν	CTE [10^{-6} $^{o}C^{-1}$]	Free [^{o}C]
IMD	60	.25	.6	420
TaN	120	.33	6.5	110
Copper	140	.34	16.6	200
Nitride	380	.33	2.25	340
Alu Cap	70	.3	23.6	390
Silicon	130	.28	3	25

5.3.7.3.3 Loading Conditions

As underlined previously, the stress field is evaluated thanks to a consideration of all process steps. Figure 93 shows the complete simulated process flow. Since all the materials are considered to be

elastic, the etching and CMP steps can be omitted, and only the stress state at the end of each deposit step is calculated. The star marked (*) operations are relative to the bond pad building and concern only the BOA model.

FIGURE 93. Simulated process flow.



5.3.7.3.4 Stress Migration Criteria

In addition to a reliable modeling which provides accurate stress and strain fields, the choice of a suitable failure criterion is one of the key factors. Two phenomena are involved in the stress induced void. The void nucleation, which is related to the creation of the initial defect, and the void growth, related to the evolution of the existing defect: The nucleation is linked to the stress level, whereas the growth is led by the stress gradient [6-7]. Therefore, both quantities will be computed and analysed aiming at quantifying the stress voiding hazard.

First of all, the void nucleation phenomenon is considered and the structures' hydrostatic pressure levels are compared. Conventionally, the hydrostatic pressure is defined as: $\sigma_{Hydro}=-(\sigma_1+\sigma_2+\sigma_3)/3$ with σ_i $i=1..3$ the principal stress components. This way, a negative amount indicates a tensile stress and the likely location of the void nucleation. On the other hand, aiming to find the privileged sites for the void growth, the stress gradient is evaluated along the M4 line. A high level of positive stress gradient allows the motion of the vacancies and empowers the growth of the voids.

5.3.7.4 Results

Width Wise Simulation Plane

In this paragraph, the stress levels between the BOA and the standard structures for the two considered line widths are compared.

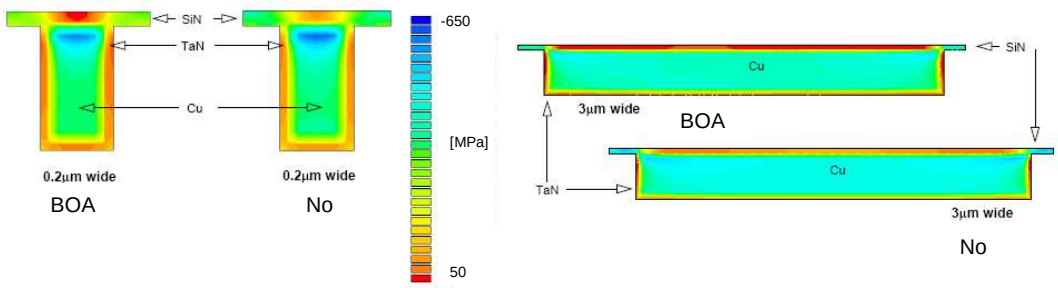


FIGURE 94. Hydrostatic stress maps in the reliability lines

Figure 94 shows the hydrostatic pressure field in the area of the tested lines. More precisely, results highlight that the stress field is not radically modified by the presence of the pad if the considered simulated plane is the width wise cross section [illegible] No BOA [illegible]he pad's impact on the stress level in the [illegible]er lines in metal 4 is a second rate parame[illegible] and the stress field is led preferably by the line itself (i.e. its layout and material properties). However, a dependence regarding the relative position of the reliability line with respect to the pad's pattern can be suspected. Generally, it can be noticed that the stress state in the materials around the copper line has common characteristics whatever the

configuration: The passivation layer is in compression in the area above the copper line, and in tension elsewhere. On the other hand, the TaN barrier is in compression. Finally, the stress in the copper lines is found to be tensile which is consistent with the stress voiding phenomenon occurrence.

A comparison of the average hydrostatic pressure in the middle of the copper lines between the two structures shows that the stress state becomes less tensile in the BOA cases. Indeed, the average hydrostatic pressures, which are equal to -465MPa and -450MPa for the narrow and the wide lines, increase respectively of 20 and 50MPa in the BOA case. Considering that a tensile stress state increases the risk of void nucleation, the pad structure would reduce the void formation phenomena in the reliability lines underneath.

Lengthwise Simulation Plane

This paragraph presents the results from the lengthwise simulation cross section.

As shown on Figure 95, the impact of the bond pad on the stress level in the Metal 4 copper line is obvious. Indeed, the stress variation at the top surface of the tested line is directly correlated with the Metal 5 layout. Regarding stress voiding hazard, the most likely sites concerning both void nucleation and growth are the ones which combine a high tensile stress state and a high stress gradient. Thus, the edge of the pad seems to be a privileged site. Some high gradient levels are also found beneath each transition between the copper in M5 and the dielectric. However, taking into account that the stress state is less tensile in this area, these locations can be considered as "secondary" privileged sites.

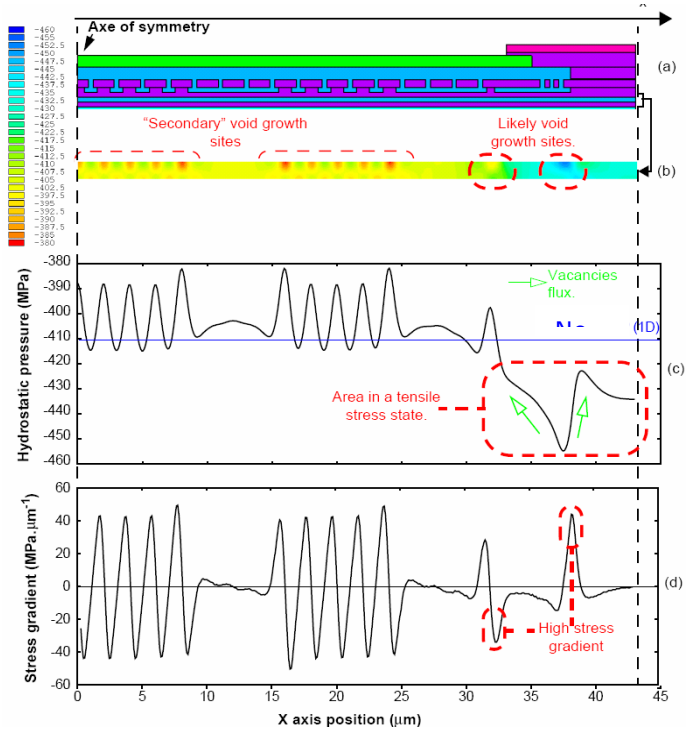


FIGURE 95. Stress figures in the reliability line (BOA case). (a) Overall view of the simulated structure (the metal layers are printed in blue). (b) Map of the hydrostatic pressure in the tested line (geometry is scaled 4 times in the y direction). (c) Hydrostatic pressure variation in the top of the tested line. (d) Gradient of the hydrostatic pressure.

5.3.7.5 Conclusion

Two dimensional simulations of the stress induced by the process steps from the Metal 4 to the passivation layer deposit have been performed. The level and the gradient of the hydrostatic pressure have been evaluated in the reliability structures with and without the bond pad above.

The results obtained from the widthwise cross section don't allow to conclude if the pad's presence could lead to major stress field differences in the tested lines. Indeed, the hydrostatic pressure in the narrow lines is dictated by the line itself, and the contribution of the pad is a lower order parameter.

However, the lengthwise modeling obviously highlights that the pad's presence impacts the stress field in the reliability structures. More precisely, two sites are found to be good candidates regarding

the stress voiding phenomena: Firstly, the bond pad edge and secondary, all the transition areas between the metal lines and the dielectric at the Metal 4 level.

Finally, this study demonstrates that the stress field, and consequently the stress voiding phenomenon, are highly dependant of the design of the above interconnect. That enables a smart management of the interconnect stress state by providing suitable design rules at the above layers.

5.3.7.6 References

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5.3.8 Mechanics and Thermo-Mechanics in Microelectronic

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5.3.8.1 Introduction

The frame of this paper is to depict mechanic and thermo-mechanic topics from the industrial point of view.
Firstly, some generalities on the microelectronic market, products and technological features are introduced. Then, some typical mechanical related applications are selected, providing quite a comprehensive overview of questions raised during technology development and through the whole manufacturing process flows. More precisely, a short illustration of how semiconductors can take advantage from strain, i.e. to boost MOS performance with the help of strain engineering. Following an example of Front-End-of-Line (FEoL), a focus on some particular Back-End-of-Line (BEoL) applications and associated failure modes is proposed. This kind of phenomena, within stress is acting as yield loss contributor are unfortunately the most widespread, since in most of the cases, stress and strain in microelectronics treat product reliability. One must be noticed that the recent introduction of advanced materials and the geometrical downscaling have turned stress induced fails into one of the major break for technology integrations.
The needs for an efficient virtual prototyping in an industrial framework are underlined. It requires compromise between both advanced experiments and simulations for a deep understanding of physics, and on the other hand the use of simplified but trustable models for technology optimization and crisis solving.

5.3.8.2 Semiconductor generalities

Year 2009, the global semiconductor sales weight 200b$, dominated by Intel Corp., which represents 15% of the market. By far behind, the competition between the top 5 companies is keen. Semiconductor company structures are evolving rapidly, the market shows abrupt speed up and drop phases, and huge R&D investments must be maintained to allow keeping in touch with technological evolutions. Inversely, it must be noticed that, chip prices for a given product functionality, decrease dramatically within a very short period of time, deprecating rapidly technologies (Figure 96). As consequences, beyond continuous fusion-buying-selling financial operations, some joint development plans are more and more carried out to divide research costs. Hence, similarly to some other industries such as automotive or aeronautics, consortiums share technological bricks, while the compounding companies remain competitors by seeking their own final customers and keeping their own product portfolios.

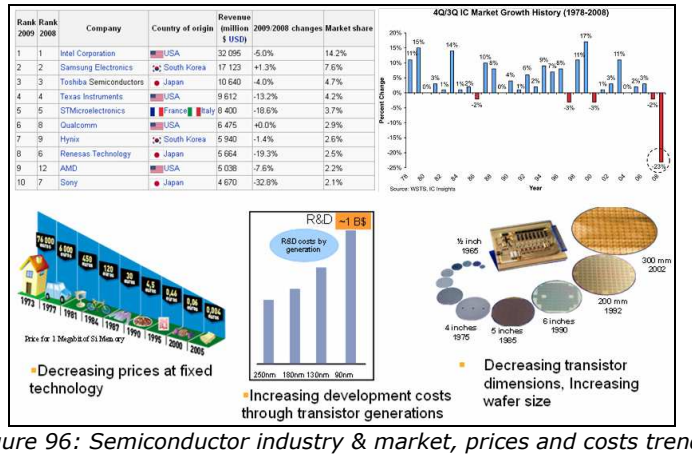


Figure 96: Semiconductor industry & market, prices and costs trends

Applications of microelectronic devices are very wide. STMicroelectronics, which is the first European semi company, is in strong position for consumer electronics, ranging from wireless, home appliances, computer peripherals, automotive electronics, etc. Besides, two major driving forces for ST's new products emerge: On the one hand energy saving concerns, and on the other hand health care applications (Figure 97). These include developments of MEMS sensors; their technological integrations into whole chip process are challenging.

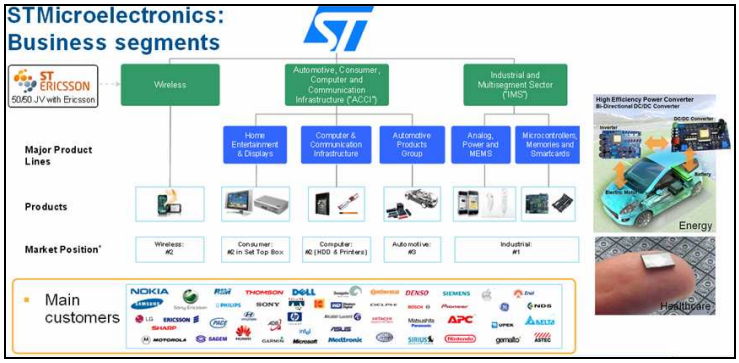


Figure 97:STMicroelectronics business segments, drivers for new products

Technological trends

At first glance, the race of improvement can be summarized in few words: "More functions, smaller dies and fewer chips".

To stick with these objectives, technological developments follow two distinct directions: The one relates to transistor downscaling, called the "Moore's law", consisting in reducing the conduction channel length, which reaches nowadays about 20nm. The other direction, called "More that Moore's law", uses integration improvements at the system level (Figure 98). More precisely it consists in playing with chip features at large scale. There are many options to complete this latter, such as 3D integration, die or wafer stacking, etc.

Finally, specific mechanical related questions are handled by the two "Moore's laws", and numerous technology breakthroughs need to be faced.

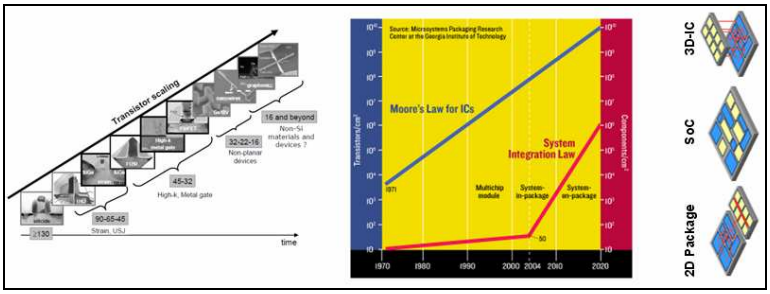


Figure 98: Technological trends, Moore's laws

Typical manufacturing flow

Making a chip consists in a huge amount of process steps. These are used to be split in two major families: The front-end, where silicon related operations are conducted to process and connect transistors at wafer level, and back-end, which corresponds to the stages from the whole wafer up to the packaged final product (Figure 99). Then, the manufactured device will be ready to be mounted to the printed circuit board and be integrated into the final customer appliance.

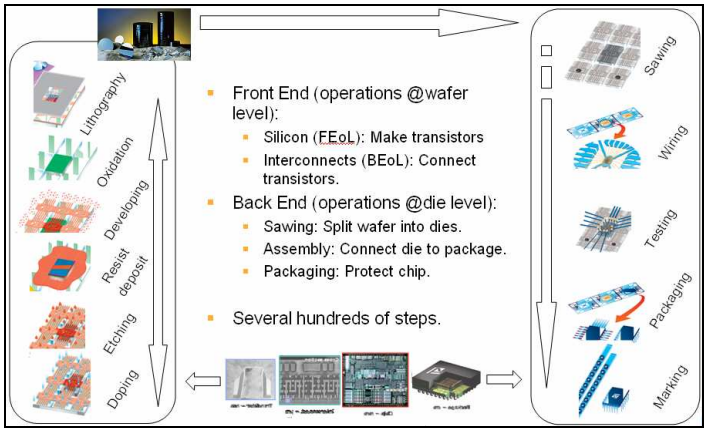


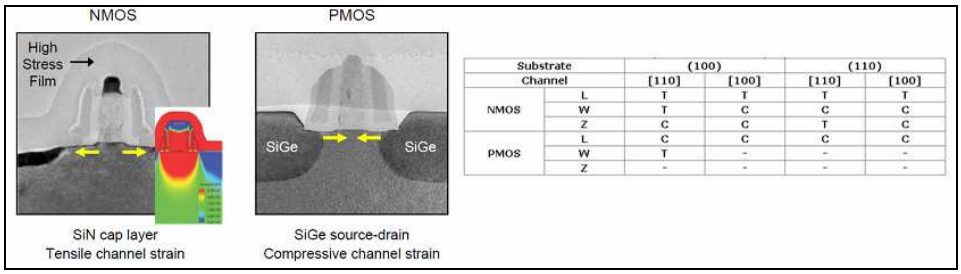
Figure 99: Typical manufacturing process flow, front-end and back-end operations

5.3.8.3 Selected mechanical challenges

In the next sections of this paper, applications are selected to illustrate some mechanical challenges of technologic developments. It must be noticed that this presentation is not aiming to be comprehensive of all concerns in which mechanics are involved. Indeed, selection is made to show, through a limited amount of examples, how strain can be either benefit or detrimental to overall performance of semiconductor products, and how to deal with them in an industrial framework.

a. **Strain engineering**

Most of the stress consequences lead to yield loss and damaging, however, strained silicon can also be used to boost electrical performance. Indeed, the electrical properties of crystal are modified by its mechanical state, due to the piezoresistive ability of silicon material (Figure 100).



Substrate		(100)		(110)	
Channel		[110]	[100]	[110]	[100]
NMOS	L	T	T	T	T
	W	T	C	C	C
	Z	C	C	T	C
PMOS	L	C	C	C	C
	W	T	-	-	-
	Z	-	-	-	-

Figure 100 Strain engineering, MOS type, substrate and channel effects, pictorial piezoresistive table for mobility boost, Compressive (C) – Tensile (T) and strain axes [7]

Several options can be used to improve the mobility in conduction channel (Figure 101). Some are based on silicon substrate orientation or strained silicon with the inclusion of dopants to change the crystalline structure. Another way is to transfer deformation of an external strained part and, by relaxation phenomena, to apply stress up to the channel. In that frame, it is obvious that the understanding of transfer mechanisms and the actual strain components knowledge is mandatory to be able to achieve performance improvement. Since the overall mobility change is a scalar combination of the strain tensor, modelling itself is an essential tool to draw relevant device layout. Furthermore, similarly to other applications, a coupled approach of experiments and simulations trials is a major tool set for optimization.

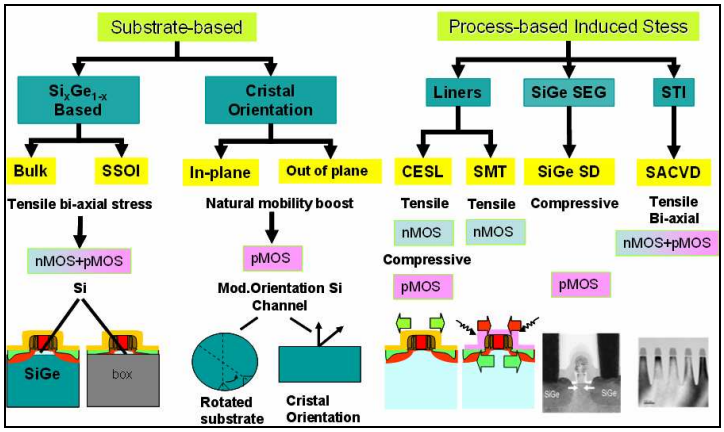


Figure 101: Strain engineering, overview of mobility booster techniques [7]

In addition to the piezoresistive effects at local scale, and knowing that stress is generated up to the silicon by BE processes, e.g. packaging processes, the global modification of device behaviours is expected. By consequence, the parameters of the electrical functions differ from the die into wafer and the packaged chip (Figure 102). More precisely, observations show that a shift in some of the parameters such as transistor matching, frequency, noise signal ratio occurs. This could lead to push the product out of specifications. This latter phenomenon is driven by a large amount of package related effects, and a smart approach is mandatory to be able to manage variability. That could be achieved either by design, material choice, or shield layers to reduce sensitivity of silicon deformation with respect to package induced stress.

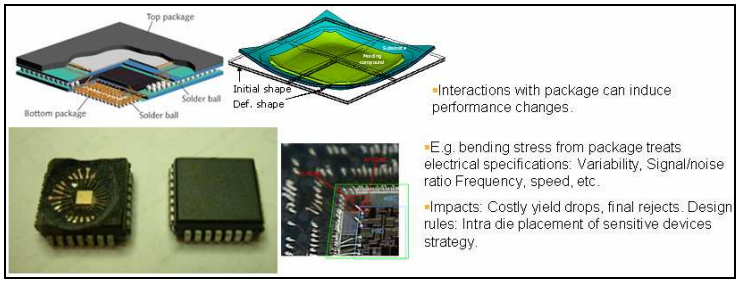


Figure 102: From local to global stressor, package induced mobility change [9], [11]

b. **Fracture mechanics in BEoL**

Similarly to critical dimension decrease in FEoL, the need for electrical performance improvements is achieved by dielectric constant value decrease of insulating materials. Hence, the k parameter is lowered through technological node evolutions. More precisely, integration of materials with lower density, which are mechanically weak, poses difficulties. Since introduction of nanometric pores is an efficient mean to lower the dielectric value, the electrical skill of advanced BEoL materials unfortunately matches its mechanical weakness (Figure 103). Hence, BEoL stack is prone to both cohesive and adhesive fracture hazards, and mechanical integrity has become a major break for integration.

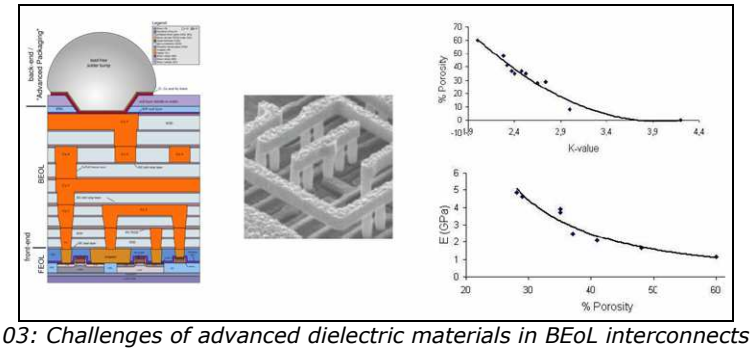


Figure 103: Challenges of advanced dielectric materials in BEoL interconnects [1], [6]

Aiming to depict the aforementioned concerns and methods to deal with, examples of the so-called "pad" architectures are chosen: The pad is the BEoL interconnect structure which is used to bridge the scales between the die and the package, and ensure the electrical connection from the FE to the BE processed parts. These regions are specially subjected to mechanical and thermo mechanical loading input from the top aluminium layer to copper/dielectric stack. Indeed, the pad structure, and consequently the whole stack below, must bear the electrical testing to check functions before packaging operations (Figure 104). Then, in case of successful test, the thermo sonic wire bonding is carried out to perform the permanent connection.

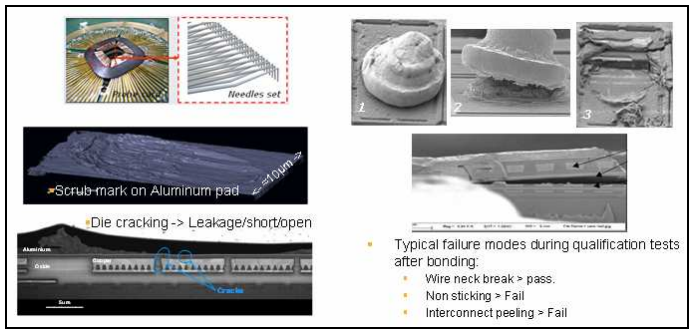


Figure 104: Mechanical stress on pads, Electrical Wafer Sort and Wire Bonding induced damages and fails [5], [6], [10]

Amongst kinds of fails induced, cohesive cracks and interfacial delamination are the most critical ones and requires design and process optimizations. Since the physics involved here are numerous and complexes, simplified but relevant modelling schemes must be determined to enable structure definition. Dedicated studies are performed to identify the most efficient framework. More precisely, contact, friction, wearing, large deformation, large strain and dynamics would require multiphysics and non linear models, which are not compatible for 3D architecture optimization. That explains why simulations and experiments are addressed in two stages: The one aiming to identify failure mechanisms and draw the relevant assumptions, the second focussing on the later findings to extract the significant features to be included for design optimization (Figure 105).
For the probing test (i.e EWS), dynamic impact features, contact geometry and loading forces with fine time sampling are achieved by explicit finite element solver. Modal analyses of Eigen frequencies and deformations complement the previous insights. Studies on pad damage also allow reproducing the aluminium scrub mark.

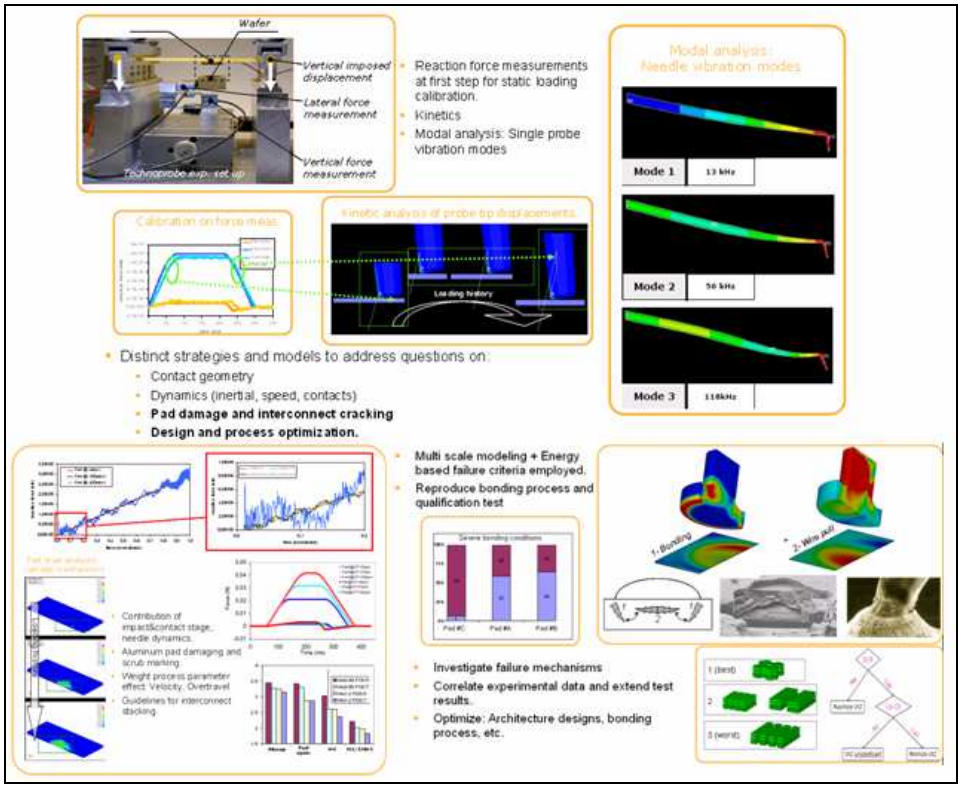


Figure 105: Investigations to optimize pad structures and equipment process parameters [5], [6], [10]

For the wire bonding process, both bonding and test cases are successively reproduced. Contact and adhesion features of the ball and the die are some of the key points driving the induced stress. As previously underlined, multi scale modelling and energy based failure index are developed and applied to reproduce the failures and draw design guidelines.
Systematically and continuously, simulation results from the whole methodologies are faced to experimental and qualification trials and complemented with dedicated measurements to check their relevance and ensure their portability trough technology node transfers.
Finally, efficient combinations of numerical and experimental methods are ready to be employed for technology development, by providing relevant support to process and design teams.

5.3.8.4 Advanced experimental methods

In addiction to these, advanced experimental and failure analysis tools are carried out with several targets, such as material properties characterization, fracture path analysis and visualisation. Three examples are described hereafter:

c. Material properties determination

Microelectromechanical systems (MEMS) like copper structures, which are suspended from substrate and can freely rotate around pivot axis, allow the reading of residual displacements. From this displacement index, it is then possible to quantify some of the strain components of the processed materials (Figure 106). This trick, complemented by Electron Backscatter Diffraction (EBSD) scans, allows understanding deeply material behaviour for several processes and patterning options by providing effects of, for example, annealing conditions, grain size features and microstructure details, line width dependence, plasticity confinement, etc.

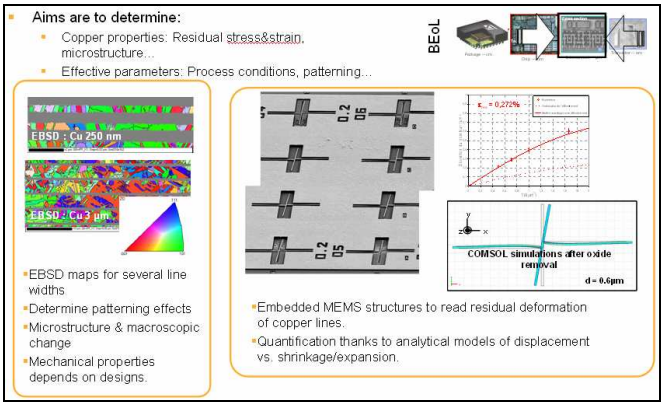


Figure 106: Material properties determination: EBSD maps and copper MEMS in BEoL [2], [4]

d. Experimental methods for fracture mechanics

The next application is related to fracture mechanics and has dual distinct aims: The one is to determine intrinsic interface properties of full sheet layers, similarly to the four point bending experiments. The second is to investigate crack features in patterned interconnect structures. Method is based on the well known nanoindentation technique. Contrary to the standard indentation technique where the tip is applied to the wafer surface, the sample is here loaded section wise, creating fracture from the initial point in the silicon up to the sample surface (Figure 107).

Analysis of the results must be completed thanks to the geometry of the remaining delamination, the computation of the loading curves, and numerical simulations of the test.

The main findings and added values of the cross nanoindentation technique are obtained on the second aforementioned target. Indeed, strong limitations remain for an accurate and reliable determination of the released energy of full sheet interfaces. In that sense, the four point bending test should still be preferred for intrinsic strength quantification purposes. However, the cross-sectional nanoindentation trials on copper/low-k structures bring rich qualitative insights on fracture mechanisms. Lessons are output on the interconnect architecture strength, providing complementary information for design purpose and to feed numerical models.

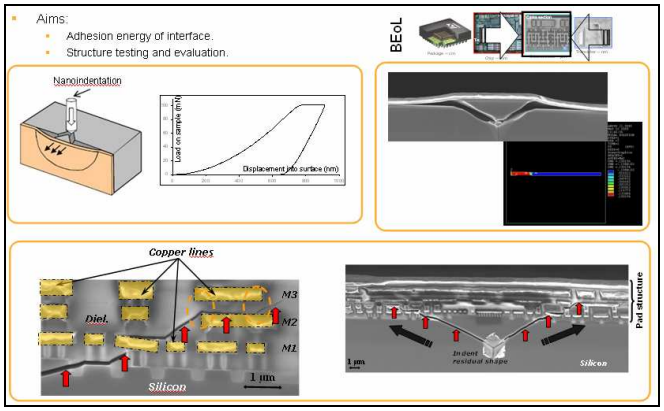


Figure 107: Experimental methods for fracture mechanics, cross-sectional nanoindentation [8]

e. Experimental methods for failure analysis

The last example of experimental methods relates to failure analysis and imaging. This technique is based on consecutive sequences of Focussed Ion Beam milling and Scanning Electron Microscopic viewing (Figure 108). Being a destructive method, three dimensional viewing of the inner parts of the die is provided by numerical post processing of the images. Amongst other benefits, this method allows an obvious depiction of the fracture features and help to understand the failure mechanisms, delaminated interfaces and drivers of crack kinking.

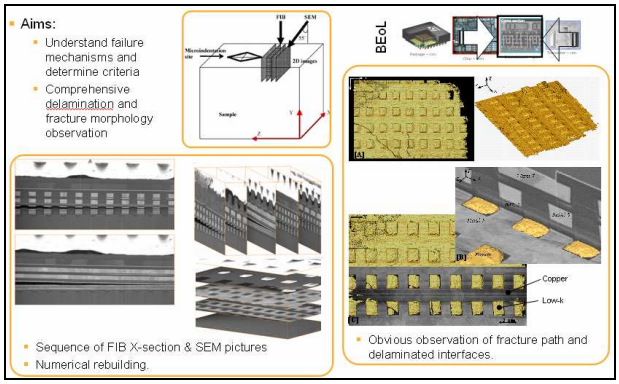


Figure 108: Experimental methods for failure analysis, 3D imaging [9]

5.3.8.5 Conclusion

This paper, dealing with mechanics and thermo mechanics in microelectronic is oriented from an industrial point of view. Semiconductor market generalities, flow of technology development, and technical trends are firstly introduced.

Then, a focus on dedicated applications to illustrate R&D requirements while introducing new technologies is proposed, and two kinds of applications are presented. The one underlines the benefits of strain engineering on electrical performances in FEoL, and the other the detrimental effects of fracture induced stress in BEoL. Example of modelling and experimental methods on pad related concerns is depicted, aiming to demonstrate that optimization strategy must be set with compromises: The knowledge of root causes and failure mechanisms requires advanced experiments and simulations to address distinct physics and draw relevant assumptions. However, to be compatible with numerical capacities and time constrains, providing technology guidelines, designing complexe architectures and tuning process parameters require a smart choice of assumptions, failure index and simulation strategy. These must be complemented by continuous validation cycle with actual silicon and dedicated test vehicles, particularly to guarantee models portability through technological nodes.

The line to stick at the competitive race is made by strong interactions with labs, manufacturers and customers. Research and long term projects, partnerships and collaborations with academic institutes are definitively mandatory, particularly for the upstream phases to be ready for future technologies.

5.3.8.6 References

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