SÉMINAIRE LAMCOS-MEGA

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Application of Tribology: Planarization of Semiconductor Electronic Materials

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ABSTRACT

Planarization refers to the fabrication silicon wafers for microelectronics such that surfaces are extremely flat. Manufacturing such electronic devices is an extremely important industry in France. Chemical-mechanical planarization, or CMP, is the most common process for integrated circuit wafer planarization. Planarization is required for accurate lithography of the circuitry. In the CMP process, the silicon wafer is pressed into a rotating compliant polishing pad flooded with a slurry of abrasive particles. Problems with CMP include slow removal rates, nonuniformity, and defects.

There have been two competing explanations of the mechanics of the material removal process during CMP. One suggests that the wafer is separated from the polishing pad by a hydrodynamic film of slurry, and polishing is done by collision of the slurry particles with the surface (erosion). The other suggestion is that the hydrodynamic effect is not strong enough to separate the wafer from the pad and the asperities of the pad rub against the wafer with entrained slurry particles (abrasion). Contrary to prior conventional wisdom of the industry, based on theoretical and experimental research, we have established convincing evidence that the latter mechanism (abrasive removal) is in force.

A model has been developed which can predict the magnitude and the trends of experimentally measured pressures in the CMP process. Only the basic formulas of solid contact mechanics and hydrodynamic lubrication theory are required. The compliant, porous nature of the pad must be considered, in contrast to prior studies which consider the pad to be rigid, smooth and impermeable. In most cases the magnitude of the fluid pressure prediction agrees with the experimental results.